

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE 1 November 1990		3. REPORT TYPE AND DATES COVERED Final August 1988–October 1990	
4. TITLE AND SUBTITLE Selective Heteroepitaxial Growth of Compound Semiconductors				5. FUNDING NUMBERS C-F49620-88-C-0106	
6. AUTHOR(S) Edward Beam and Yung-Chung Kao AFOSR-TR-90-1166				8. PERFORMING ORGANIZATION REPORT NUMBER 08-90-53	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) TEXAS INSTRUMENTS INCORPORATED CENTRAL RESEARCH LABORATORIES P. O. BOX 655936 DALLAS, TEXAS 75265				10. SPONSORING/MONITORING AGENCY REPORT NUMBER 2305/C1	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) AFOSR/NE Bldg. 410 Bolling AFB, DC 20332					
11. SUPPLEMENTARY NOTES					
12. DISTRIBUTION/AVAILABILITY STATEMENT Distribution/Availability Statement Distribution unlimited.					
13. ABSTRACT (Maximum 200 words) The effect of reduced growth area on the lattice mismatch accommodation of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ and GaAs/Si grown by molecular beam epitaxy (MBE) has been studied with cross-sectional transmission electron microscopy (XTEM) and cathodoluminescence (CL). Results indicate that the use of step-composition grading and linear-composition grading are particularly effective when combined with reduced growth areas and $\text{In}_x\text{Ga}_{1-x}\text{As}$ compositions up to $x = 0.25$. Blanket areas with the same composition grading techniques exhibited randomly distributed threading dislocation-free regions approximately 30 μm in diameter, which were bounded by high-density dislocation pile-ups. $\text{In}_x\text{Ga}_{1-x}\text{As}$ compositions greater than $x = 0.25$ exhibited higher threading defect densities. This is attributed to the breakdown of the layer-by-layer growth mode to a three-dimensional growth mode. Improvements in the quality of reduced-area GaAs/Si was not realized. Large densities of sessile threading dislocation were observed and are attributed to dislocation interactions during the early stages of misfit accommodation.					
14. SUBJECT TERMS Selected Area Growth GaAs/Si Defect Density Reduction Reduced Area Growth $\text{InGaAs}/\text{GaAs}$				15. NUMBER OF PAGES 55	
				16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT Unclassified		18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified		19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	
				20. LIMITATION OF ABSTRACT SAR	

**FINAL TECHNICAL REPORT
FOR
SELECTIVE HETEROEPITAXIAL GROWTH
OF COMPOUND SEMICONDUCTORS
CONTRACT NO. F49620-88-C-0106
August 1988—October 1990**

Prepared for
Air Force Office of Scientific Research
Bolling AFB, DC

1 November 1990

Prepared by
Texas Instruments Incorporated
Central Research Laboratories
P. O. Box 655936
Dallas, Texas 75265

TABLE OF CONTENTS

Section	Title	Page
	SUMMARY	1
I	INTRODUCTION	3
	A. Previous Work on Defect Reduction	3
	1. Problems with Misfit Accommodation	3
	2. Large-Area Defect Reduction	4
	3. Reduced-Growth Area Defect Reduction	5
	B. This Program's Approach to Defect Reduction	6
	1. Choice of Materials Systems	6
	2. Hybrid Reduced-Area Growth Technique	6
	3. Device Considerations	7
II	EXPERIMENTAL PROCEDURES	8
	A. Patterned Growth Structures and Processing	8
	1. GaAs Substrates	9
	2. Si Substrates	10
	B. MBE Growth Procedures	11
	C. Materials Characterization	13
III	THE InGaAs/GaAs SYSTEM	14
	A. Homogeneous Growth	14
	B. Composition-Graded Growth	18
	1. Reduced Area Growth with Step-Composition Grading	18
	2. Reduced-Area Growth with Linear-Composition Grading	22
	3. Discussions of Composition Graded Growth Results	24
IV	THE GaAs/Si SYSTEM	32
	A. Large-Area (Blanket) Growth	32
	B. Reduced-Area Growth	34
V	RECOMMENDATIONS FOR ADDITIONAL STUDY	51
	A. The InGaAs/GaAs System	51
	B. The GaAs/Si System	51
	REFERENCES	52



Accession For	
NTIS GRAB	<input checked="" type="checkbox"/>
DTIC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By	
Date	
Availability Code	
Dist	
A-1	

LIST OF ILLUSTRATIONS

<i>Figure</i>	<i>Title</i>	<i>Page</i>
1	Misfit Dislocation Generation Processes When the Substrate Dislocation Density is Low	4
2	Schematic Description of Defect Density Reduction Techniques that have been Employed for Lattice Mismatched Heteroepitaxy	5
3	Various Methods for Reduced-Area Epitaxial Growth	8
4	Process Sequences for Cantilever Mask Structures, (a) InGaAs/GaAs Etch-Down Structure, m(b) GaAs/Si Stack-Up Structure	9
5	Scanning Electron Micrograph of Cantilever Shadow Mask Patterned In _{0.20} Ga _{0.80} As Islands in a GaAs Substrate. The In _{0.20} Ga _{0.80} As islands are well isolated along both <110> substrate directions.....	10
6	Cross-Sectional Transmission Electron Micrograph of GaAs/Si Prepared by Cantilever Shadow Masking	11
7	Mask Layout for Selected Area Growth	12
8	Growth Temperature Profile for the Two-Step GaAs Grown on Si Including Thermal-Strained Superlattices and AlGaAs Cap In Situ Annealing Processes	13
9	Cross-Sectional Transmission Electron Microscope (XTEM) Micrograph of Direct Growth of In _{0.07} Ga _{0.93} As on 4- μ m-Wide GaAs Mesa	15
10	XTEM Micrograph of Direct Growth of In _{0.20} Ga _{0.80} As in a 10- μ m-Wide GaAs Trench	16
11	XTEM Micrograph of Direct Growth of In _{0.20} Ga _{0.80} As With an Intermediate 5-Period In _{0.20} Ga _{0.80} As/GaAs Strained-Layer Superlattice in a 10- μ m-Wide GaAs Trench	17
12	XTEM Micrograph of a Two-Layer Step-Composition-Graded Epilayer on a 10- μ m-Wide GaAs Mesa	19
13	XTEM Micrograph From a Four-Layer Step-Composition-Graded Epilayer on a 10- μ m-Wide GaAs Mesa.	20
14	XTEM Micrograph From the Same Growth Structure as Figure 18 (but from a Large-Area Blanket Region).....	21
15	XTEM Micrograph From the Same Growth Structure as Figures 8 and 9 in a 30- μ m-Wide Trench.....	23
16	XTEM Micrograph From a Five-Layer Step-Composition-Graded Epilayer in a 10- μ m-Wide GaAs Trench.....	24
17	XTEM Micrograph of Threading Dislocations in the Top Two Layers for the Same Growth Structure as in Figure 20	25
18	XTEM Micrograph From a Linear-Composition-Graded Epilayer to In _{0.25} Ga _{0.75} As in a 10- μ m-Wide GaAs Trench	26
19	XTEM Micrograph From a Linear-Composition Graded Epilayer to In _{0.53} Ga _{0.47} As in a 10- μ m-Wide GaAs Trench	27
20	Schematic Description for the Formation of High-Density Dislocation Pile-Up Centers in Large-Area Lattice-Mismatched Epilayers (i.e., $l \ll L$)	28
21	Edge Nucleation of Glide Dislocation Quarter-Loops for Misfit Accommodation	29

LIST OF ILLUSTRATIONS (Continued)

<i>Figure</i>	<i>Title</i>	<i>Page</i>
22	The Effect of Reduced Area Growth Size on Dislocation Dynamics	30
23	Cross-Sectional TEM Micrograph of GaAs/Si Prepared Using Thermal Superlattice Layers and Followed by an AlGaAs Cap Anneal	33
24	Cross-Sectional TEM Micrograph of the Transition From Single-Crystal to Polycrystalline Growth in Patterned GaAs-on-Si	35
25	SEM Micrograph of GaAs Grown in a 50- μ m-wide Si Trench	36
26	Cross-Sectional Micrographs of GaAs Grown Over Etch-Defined Si Trenches	37
27	(a) XTEM Micrograph of GaAs Grown on 3- μ m-wide Si Mesa, (b) Tracing of This Micrograph	38
28	Defect Structure of As-Grown GaAs at the Sidewall of a 100- μ m-wide Si Mesa	39
29	Various Sized Cantilever Shadow Mask Patterned GaAs/Si Structure.	40
30	XTEM Micrograph From a GaAs Epilayer Grown by the Two-Step Method in a 10- μ m-wide Cantilever Shadow Mask Patterned Si Trench	41
31	XTEM Micrograph From a GaAs Epilayer Containing Two 5-Period SLSs inside a 10- μ m-wide Cantilever Patterned Si Trench	42
32	XTEM of the Same Growth Structure as Shown in Figure 31 (But in a 5- μ m-wide Trench)	43
33	XTEM Micrograph From a Portion of a GaAs Epilayer Containing Two AlGaAs Cap Layers Inside a 10- μ m-wide Cantilever Patterned Si Trench	43
34	XTEM Micrograph From a GaAs Epilayer Containing Three AlGaAs Cap Layers and a 5-Period SLS in a 10- μ m-wide Cantilever Patterned SI Trench	45
35	Plan-View TEM Image From a Trench Region of the Same Growth Structure as Shown in Figure 34	45
36	Cathodoluminescence Images From Various Sized Growth Areas for the Growth Structure Shown in Figure 34	46
37	XTEM Micrographs From a GaAs Epilayer Containing One AlGaAs Cap Layer and Three 5-Period SLSs inside a 10- μ m-wide Cantilever Patterned Si Trench	47
38	XTEM Micrographs Under Several Imaging Conditions of a Group of Dislocations from the Same Growth Structure as Shown in Figure 37	48
39	Schematic Diagram Showing (a) the Generation of a Threading Dislocation from the Interaction of Two Misfit Accommodating Dislocations, and (b) the Blocking Affect of these Dislocations Threading through the Glide Planes of other Dislocations	50

**FINAL TECHNICAL PROGRESS REPORT
FOR SELECTIVE HETEROEPITAXIAL GROWTH
OF COMPOUND SEMICONDUCTORS**

CONTRACT NO. F49620-88-C-0106

August 1988—October 1990

SUMMARY

The objective of this program was to develop the understanding required to minimize the defects that arise during reduced-area heteroepitaxial growth. Emphasis was placed on the study of the large lattice mismatched materials systems, GaAs/Si and $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$. The GaAs/Si system has an abrupt change in crystal composition and lattice spacing at the substrate/epilayer interface. The $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ system allows a composition variation for distribution of the lattice mismatch within the epilayer thickness; this system is also attractive for the subsequent growth of a lattice-matched InP epilayer over $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{GaAs}$.

The first portion of this program involved the development of the techniques for molecular beam epitaxial growth of materials on selected areas on a substrate. These selected-area growth techniques were used to produce lattice-mismatched structures for defect studies. Cross-sectional transmission electron microscopy (XTEM), x-ray diffraction, and cathodoluminescence (CL) were used to characterize the defect structures. Specific accomplishments and findings from this work are summarized below.

- Initial studies of GaAs grown on small Si pedestals showed an increased epilayer defect density caused by interaction between the GaAs grown on the top and sides of the pedestal.
- A *cantilever* shadow masked growth technique was developed to overcome the sidewall growth problem. The resulting relatively planar structure will facilitate device processing.
- Direct growth of $\text{In}_x\text{Ga}_{1-x}\text{As}$ with $x \geq 0.20$ on GaAs resulted in a very high density of threading dislocations, which were aligned nearly perpendicular to the growth interface. Strained-layer superlattices were not effective for dislocation reduction.
- Both step- and linear-composition graded growth of unpatterned $\text{In}_x\text{Ga}_{1-x}\text{As}$ (up to 25% In) on GaAs substrates produced small regions ($\sim 30\text{-}\mu\text{m}$ wide) of low defect density. These low-defect regions were bordered by regions containing a high density of threading dislocations, resulting from dislocation interactions during the misfit accommodation process.
- Reduction of patterned growth area to less than $30\text{ }\mu\text{m} \times 30\text{ }\mu\text{m}$, combined with composition grading, resulted in the propagation of misfit dislocations to the edges of the epilayer. This effect is attributed to reduction of the distance for gliding misfit forming dislocation movement to less than the dislocation interaction mean-free-path.
- Step-composition graded growth of $\text{In}_x\text{Ga}_{1-x}\text{As}$ compositions higher than 25% In resulted in a large density of threading dislocations. This increased

dislocation density is attributed to a change from two-dimensional layer-by-layer growth to three-dimensional island-type growth.

- The majority of the residual threading dislocations in the high-In step-composition graded epilayers had Burgers vectors parallel to the growth surface. As such, these dislocations cannot be driven to the edge of the growth areas using misfit stress.
- Linear-composition graded InGaAs layers had less phase separation than step-composition graded layers. Also, the defect density of linearly graded $\text{In}_x\text{Ga}_{1-x}\text{As}$ with $x \geq 0.25$ was considerably lower than that for the step-composition layers. Both of these effects may be caused by better preservation of the two-dimensional growth mode with the gradual composition change.
- The use of a lower growth rate and growth temperature may be useful for improving the quality of higher-In composition graded layers. Migration-enhanced epitaxy may preserve the two-dimensional growth mode.
- Overall, a significant defect density reduction was not obtained in patterned GaAs/Si. Regions approximately $2\text{ }\mu\text{m}$ from the reduced area growth edges exhibited a reduced defect density, but the defect density in the central regions was comparable to that of blanket grown epilayers.
- Incorporation of in situ annealing techniques produced similar results as those on large-area blanket GaAs/Si layers. Patterned growth had little affect on dislocation density, except near the GaAs edges.
- Use of strained-layer superlattices in patterned GaAs/Si has little affect because of the high densities of threading dislocations, which were not lying on $\{111\}$ type glide planes. These immobile dislocations act to block the movement of dislocations that do lie on glide planes.
- Improvement of the perfection of patterned GaAs/Si will likely most benefit from changes in the initial stage of growth, such as the use of a low growth-rate technique (for example, migration-enhanced epitaxy). Prevention of substantial dislocation interactions would minimize dislocations that reorient out of the $\{111\}$ glide planes during growth.

SECTION I

INTRODUCTION

The cointegration of various devices such as linear, digital, microwave, optoelectronic and/or photonic devices on a single wafer could improve the intrinsic performances of these devices by eliminating the deleterious effects of parasitic capacitances.¹ Integration of multimerials on a common substrate is very attractive for development of such multifunctional devices. Multimerials on a substrate would permit specific device types to be made with the optimum material, rather than compromising the performance of all the device types by the use of a single materials system. Unfortunately, significant problems exist with respect to large lattice-mismatched heteroepitaxy required for multimerials integration. To make this approach feasible, particularly for the case of minority-carrier-based devices, significant reductions in defect densities are required in lattice-mismatched layers. The primary objective of the present research program has been to evaluate the use of selective growth for reducing defect densities in lattice-mismatched materials systems.

A. PREVIOUS WORK ON DEFECT REDUCTION

1. Problems with Misfit Accommodation

The majority of the defects in lattice mismatched heteroepitaxial layers are a result of the inefficient misfit accommodation processes during growth. Figure 1 shows a series of schematics for various situations that may occur during large lattice mismatched epilayer growth on substrates with low dislocation densities. For the ideal situation [Figure 1(a)], as growth of a mismatched layer exceeds the critical thickness for misfit dislocation nucleation by half-loop formation, for each misfit dislocation that is required at the heterointerface one misfit dislocation is nucleated and propagates to the interface and terminates at the edge of the wafer. This situation in practice is not readily achieved. The probability for dislocation interaction and multiplication is directly dependent on substrate size and lattice mismatch,² and only when very small lattice mismatches and small substrate dimensions are used will the dislocations propagate to the growth edges. Another problem often observed is redundant nucleation of dislocations. This is illustrated in Figure 1(b). In this case, for every misfit dislocation that is required, several are nucleated across the width of the surface. As these dislocations propagate toward the substrate-epilayer interface, they impinge upon one another. When the Burgers vectors are favorable, the dislocations can interact to annihilate. However, when the Burgers vectors of two impinging dislocations do not sum to zero, the dislocations will interact to produce a threading dislocation segment. Again, the extent of defect formation by this mechanism should increase with increasing lattice mismatch and substrate dimension. Finally, a large density of threading dislocations can result when epitaxial growth occurs by three-dimensional (island) growth and subsequent coalescence. This mechanism is depicted in Figure 1(c). In this case, when growth occurs by the formation and growth of isolated islands on the surface, as the thickness of each individual island exceeds the critical thickness for misfit dislocation formation, arrays of misfit dislocations will be formed in each island. As growth proceeds and these islands coalesce, since the dislocations can not terminate within the crystal, they must either interact to annihilate, to form a

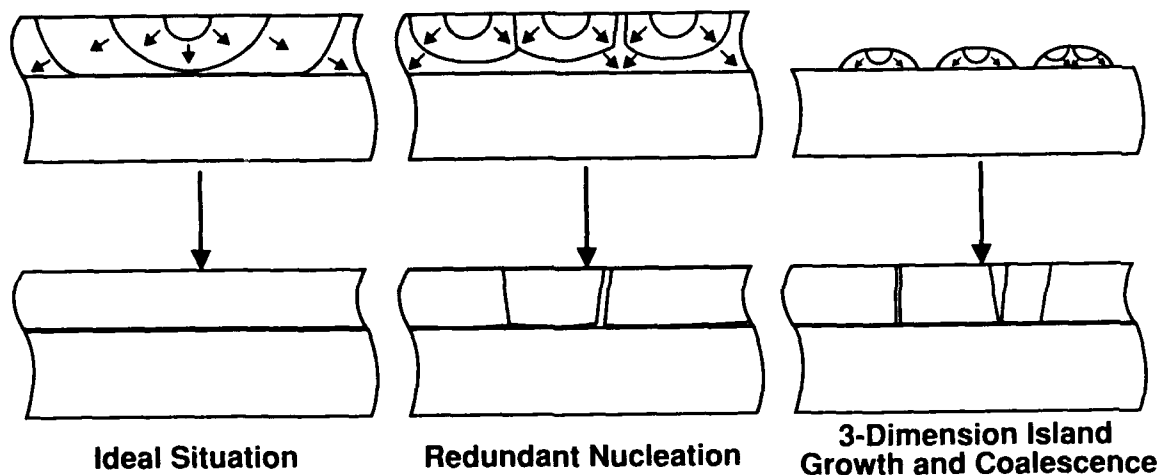


Figure 1
Misfit Dislocation Generation Processes When the Substrate Dislocation Density is Low

third dislocation, or propagate to the free surface. This mechanism for defect formation is particularly relevant for the case of large lattice mismatches and when the crystal structure between substrate and epilayer is different, i.e., GaAs/Si.³ Finally, high densities of defects can be generated in epilayers because of thermal-expansion mismatch stresses. As a sample is cooled from the growth temperature, in materials systems with large thermal-expansion mismatches, sufficient stresses can develop to produce plastic deformation and, subsequently, a large density of threading dislocations. These stresses are dependent on substrate size.

2. Large-Area Defect Reduction

To improve the efficiency of the misfit accommodation process and/or to reduce the threading dislocation densities in mismatched heteroepitaxial layers, a number of approaches have been employed. Figure 2 provides an overview of the most promising techniques. A large group of experiments have been focused on strain and/or composition-grading techniques. With these techniques, the lattice mismatch is distributed through buffer layers of finite thicknesses. Several attempts have been made to distribute the mismatch by linearly grading the composition through buffer layers^{4,5} or by discrete composition steps through buffer layers.^{4,6} These experiments were confined to blanket epitaxial layers. The basic principle behind these composition-grading approaches is to reduce the number of misfit dislocations required at an abrupt heterointerface. By composition grading, the number of misfit dislocations that are nucleated at any one interface is reduced; therefore, these fewer dislocations have a better chance of gliding to the interface without interaction. Also, the threading dislocations, which are generated during the growth of the buffer layer, may be bent back into the next step-composition-graded interface or continuously during linear composition grading. This approach, when applied to large substrate dimensions, implies that the dislocations must glide extensive distances during formation to reach the edges of the substrate. It has been observed that this situation does not readily occur in blanket epilayers, rather, small regions are observed be relatively free of threading dislocations and are surrounded by high-density inclined dislocation centers (HDIDs).⁶

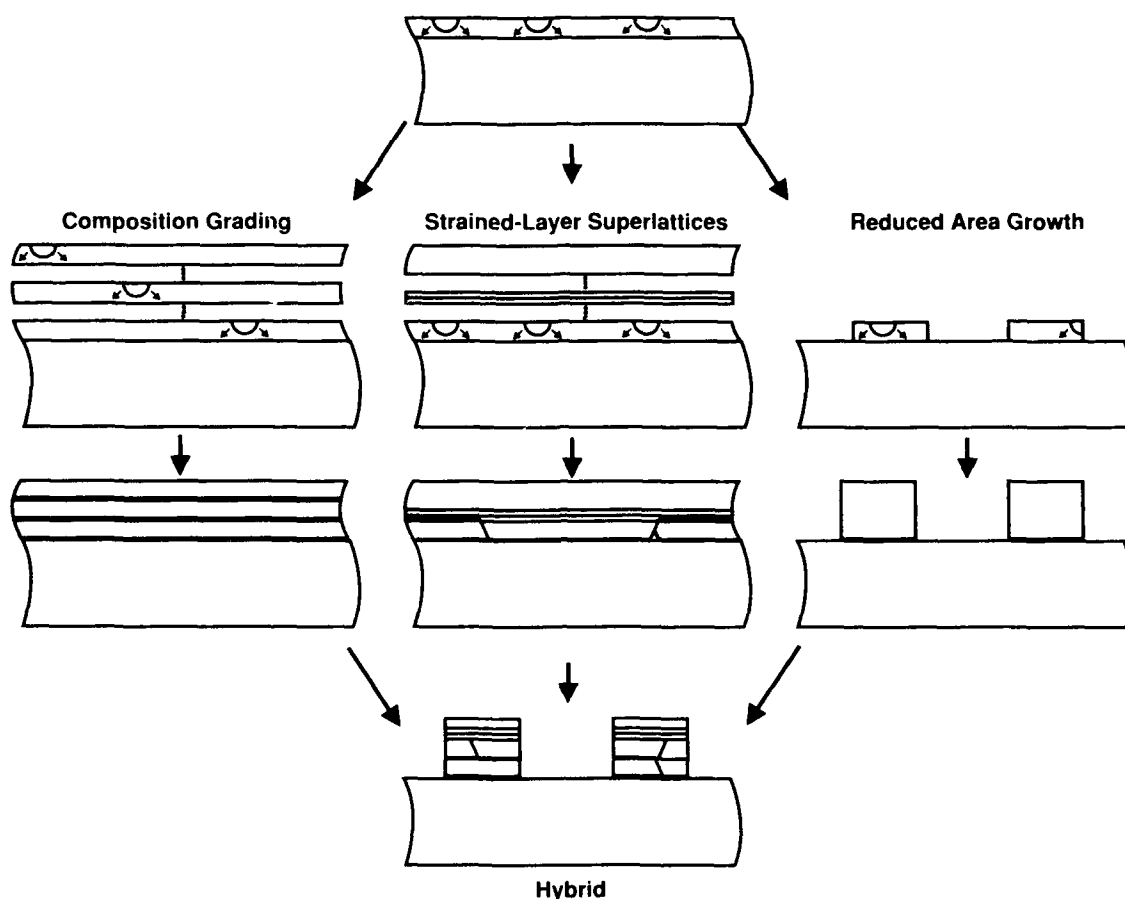


Figure 2
Schematic Description of Defect Density Reduction Techniques that have been Employed for Lattice Mismatched Heteroepitaxy

Another approach that has received considerable attention is the use of strained-layer superlattices for *dislocation filtering*.^{2,7-9} In this case, intermediate multiple strained-layers are used in an attempt to bend threading dislocations into the strained-layer interfaces and thus to the boundaries of the epilayer. For this type of solution, the threading dislocation nucleation problem that occurs during the misfit accommodation process is not addressed; rather, attempts are made to drive these resultant dislocations into interfaces of the strained-layer superlattice. Again, in this case, for a large sample dimension this implies that the dislocations must be driven to very large extents to reach the sample edges, or favorable dislocation interactions must be obtained. As such, there is a narrow range for initial dislocation densities for which this method is effective.⁸

3. Reduced-Growth Area Defect Reduction

Recently, the use of reduced growth areas has been shown to be very effective for reducing misfit and threading dislocation densities in the material systems $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ and $\text{Si}_x\text{Ge}_{1-x}/\text{Si}$ when the lattice mismatches and epilayer thicknesses are relatively small.¹⁰⁻¹² The improvement in defect density is attributed to the shortening of the misfit dislocation lengths required in reduced growth areas, a reduction of fixed

dislocation sources within a small area compared to a large area, and strain relief at the mesa edges. The application of this technique to large lattice mismatches and thick epilayers has not been reported for these materials systems. Reduced area growth of GaAs/Si has been reported^{13,14}; however, significant improvements in defect density has not been demonstrated. The problem with this system is that the lattice mismatch must be accommodated at a single interface. Materials system where intermediate composition transitions can be used may prove to be more successful.

B. This Program's Approach to Defect Reduction

1. Choice of Materials Systems

Two situations are encountered with the latticed mismatched heteroepitaxy of semiconductor materials. In one case, the crystal structure of the substrate and epilayer may not be the same. In this situation, the interface between the epilayer and substrate is abruptly defined. In the other case, the crystal structure of the substrate and epilayer are the same and alloys between the two materials can be formed. The resulting heterointerface can be made with various levels of abruptness. This is advantageous as it provides an additional degree of freedom for defect-reduction possibilities.

To evaluate the effects of reduced-area growth for defect-density reduction in lattice-mismatched heteroepitaxial layers more generally, we have chosen materials systems for the study of both types of interfaces. The GaAs on Si system was chosen as the model system where the crystal structure differs between substrate and epilayer. In this case, the lattice mismatch is 4.2%. The $\text{In}_x\text{Ga}_{1-x}\text{As}$ on GaAs materials system was chosen for the case where the crystal structure is continuous across the interface. $\text{In}_x\text{Ga}_{1-x}\text{As}$ compositions as high as $x = 0.53$ were chosen for this work. This particular composition is latticed matched to InP, and, thus, if high-quality $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ on GaAs layers can be produced, the potential for InP on GaAs cointegration might be more effectively realized.

2. Hybrid Reduced-Area Growth Technique

Our approach to the reduction of defect densities in latticed-mismatched heteroepitaxial layers has been the synergy of conventional defect-density reduction schemes with reduced area growth, and is depicted schematically at the bottom of Figure 2. We have combined the use of composition-grading growth techniques and/or strained-layer superlattice *dislocation filtering* with selected area growth. This hybrid technique eliminates the large distances that misfit dislocations must acquire during the misfit accommodation process. For this reason, effects of the composition-grading and dislocation-filtering techniques should be more effectively realized, since the probability of dislocation interactions should be reduced with reduced growth area. For the $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ system, we have explored the use of strained-layer superlattices and both step- and linear-composition grading with reduced growth areas for defect-density reduction. For the GaAs/Si materials system, we have examined the effects of strained-layer superlattices and in situ annealing techniques with reduced growth areas.

3. Device Considerations

For multimaterials cointegration to be practical for consideration in device applications, not only must the defect densities be lowered, but the resulting growth structures must be compatible with fabrication technologies. Two important constraints related to this issue are usable device fabrication area and the ability to planarize the surface after epi-growth. A lower limit to the area required for the fabrication of individual devices is on the order of $3\text{ }\mu\text{m} \times 3\text{ }\mu\text{m}$; however, larger areas would be preferred. The separation between the multimaterials areas is also a serious concern and can influence planarizability. We have considered these issues with the development of the reduced-area growth structures that we have used for defect-reduction studies.

SECTION II EXPERIMENTAL PROCEDURES

A. PATTERNED GROWTH STRUCTURES AND PROCESSING

Considerable attention has been focused on the use of selective epitaxy,¹⁵ growth on oxide- or nitride-patterned wafers,¹⁶ growth on etch defined pedestals,^{10,11} growth through mechanical shadow masks,^{17,18} growth in undercut trenches^{19,20} or postgrowth patterning²¹ for realizing defect-density reduction with reduced-area growth. Figure 3(a through f) shows schematic illustrations for these various techniques. Unfortunately, there are significant problems with these techniques for MBE-grown epilayers. Selective epitaxy is difficult with MBE, requiring high growth temperatures and low growth rates. Sidewall growth interactions in material grown on oxide- or nitride-patterned substrates often exhibits severe degradation at the patterned growth edges. Growth on etch-defined mesas results in very nonplanar surfaces, and the growth morphology often exhibits facets at the epilayer edges. Growth in undercut trenches is effective for only one orientation in III-V semiconductors because of the anisotropic nature of the etching of these materials. MBE growth through mechanical shadow masks can alleviate some of these problems, but mask generation and precise growth area positioning is difficult. Finally, postgrowth etch patterning can relieve some of the built-up thermal-expansion stresses, but it does not address the issue of defect elimination during the growth process.

For the work performed in this research program, we have employed the use of growth in undercut trenches, nonundercut trenches, growth on etched defined mesas, and we have developed a new type of reduced area growth technique that we term *cantilever shadow masked growth*.²² A schematic illustration of the structure of this new patterning technique is shown in Figure 3(f). The primary advantage of this technique is that shadowed growth can be obtained in all orientations relative to a GaAs substrate surface, and

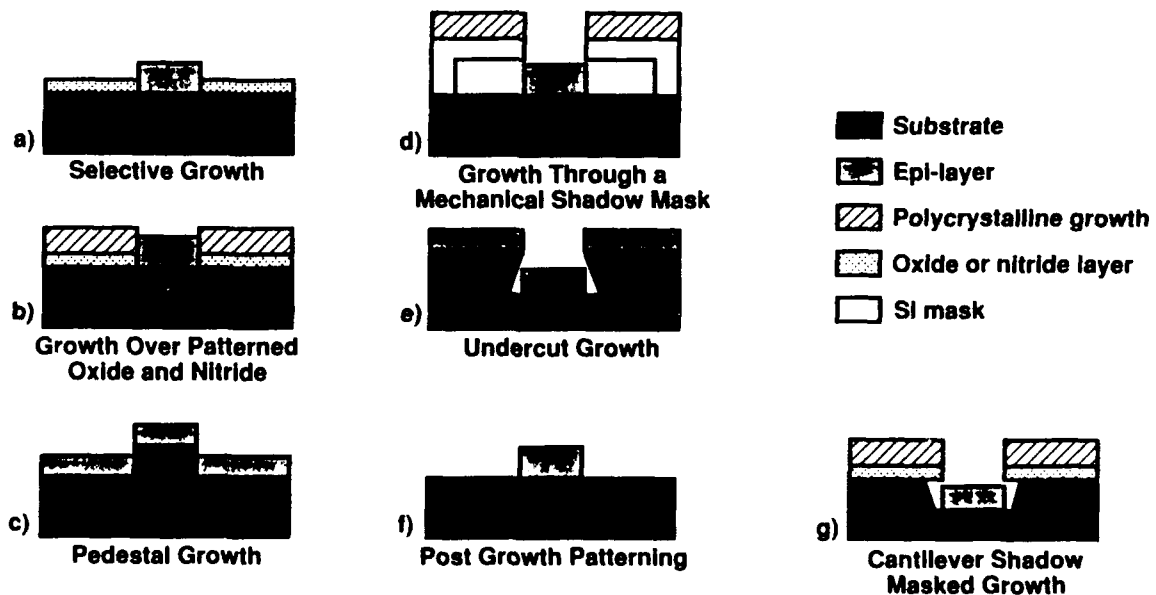


Figure 3
Various Methods for Reduced-Area Epitaxial Growth

02636

that this technique can also be applied to Si substrates. In addition, the use of this technique results in precisely positioned growth areas; can be more readily planarized than other techniques; eliminates sidewall growth interactions; and, when optimized, can produce planar growth profiles.

The details for the processing of the patterned growth structures used in this study for GaAs and Si substrates are now described.

1. GaAs Substrates

The undercut trench and etch defined mesa structures were formed on the same GaAs substrates by etching through windows in silicon-nitride-patterned GaAs substrates with 1:8:10 $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$. The substrates used for this study were 2 inch (001) misoriented 2 degrees off toward the $\langle 011 \rangle$ direction. After removal of the nitride mask with buffered HF, these substrates were loaded into the MBE reactor. This structure was useful for studying the material grown on top of the mesas and the material grown within the undercut trenches. However, the undercut geometry was possible in only one of the $\langle 110 \rangle$ directions. To circumvent this problem, we have used the *cantilever* shadow masked structure shown in Figure 3(f). Figure 4(a) shows the process flow for the cantilever shadow masked growth of InGaAs on reduced areas of a GaAs substrate. First, a silicon-oxide or silicon-nitride film is deposited on the wafer surface. Windows are opened in this masking layer using conventional photolithographic techniques; thereby, the spatial position of the growth areas can be precisely controlled. Etching is then performed on the oxide- or nitride-patterned wafers, such that the masking layer is undercut

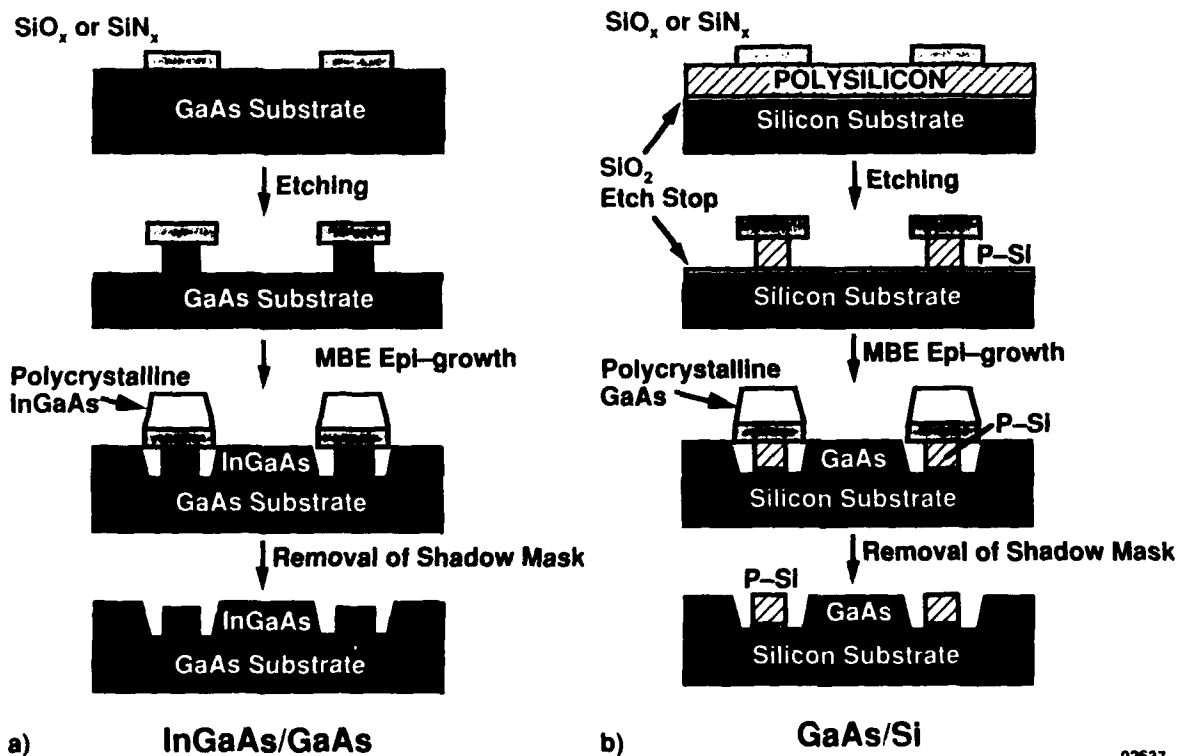


Figure 4
Process Sequences for Cantilever Mask Structures, (a) InGaAs/GaAs Etch-Down Structure,
(b) GaAs/Si Stack-Up Structure



InGaAs/GaAs (After Removal of Mask Material)

Figure 5
Scanning Electron Micrograph of Cantilever Shadow Mask Patterned $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ Islands in a GaAs Substrate. The $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ islands are well isolated along both $\langle 110 \rangle$ substrate directions.

and the bottom etch surface remains planar. The etchant that we have used for GaAs is: $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$, 1:8:10.

Although this etchant is highly anisotropic, undercutting of the nitride masking layer is possible in both $\langle 110 \rangle$ substrate directions. In addition, this etchant is very well suited for producing a flat trench bottom. After the etching step, wafers are rinsed thoroughly with deionized water and then loaded in the MBE reactor. After MBE growth, the nitride masking layer and the polycrystalline material deposited on it can be removed by dissolution in buffered HF. Figure 5 shows an SEM micrograph of a series of InGaAs islands on GaAs that have been produced by this cantilever shadow mask technique. In this case, the nitride layer and the polycrystalline overgrowth have been removed. The thickness of the InGaAs islands is $3\text{ }\mu\text{m}$. These islands are very well isolated from the GaAs sidewalls, and exhibit relatively planar surface morphologies.

2. Si Substrates

Etch-defined mesas and nonundercut trenches were produced on two-inch diameter Si substrates having their [001] orientation tilted 4 degrees toward the [110] direction. These wafers were cleaned using conventional degreasing/chemical cleaning before deposition of an 800-nm SiO_2 layer. The oxide was then lithographically defined to serve as the mask for etching. Etching was performed using reactive ion etching followed by the planar etch $\text{HF}:\text{HNO}_3:\text{HC}_2\text{H}_3\text{O}_2$, 2:15:5. The oxide was then removed prior to loading into the MBE reactor. Figure 4(b) shows the process flow which was used for the preparation of the cantilever masked growth structures. First, a sandwiched $\text{SiO}_2/\text{poly-Si}/\text{SiO}_2$ layer is deposited on the Si wafer surface. Windows are then opened in the top

oxide masking layer using conventional photolithographic techniques. Since the typical poly-Si thickness is 3- to 4- μm thick, reactive ion etching is used first to etch the poly-Si without undercutting. Conventional Si isotropic etching is then used to undercut the oxide masking layer. The bottom thin oxide serves as an etch stop such that the crystalline Si surface remains planar. After patterning, the thin oxide is stripped and a protective oxide layer is grown before loading into the MBE system. Figure 6 shows an XTEM micrograph of an as grown GaAs epilayer on a cantilever patterned Si substrate. The growth is completely free of sidewall growth interactions.

The selected area patterning mask that was used for the preparation of the growth structures was designed to simplify XTEM sample preparation and to avoid problems of feature size identification. As shown in Figure 7, the mask consists of four quadrants, three of them containing patterns of vertical bars, squares, and horizontal bars (identical to vertical bars but rotated 90 degrees). One quadrant is left unpatterned for blanket area growth comparisons. Each patterned quadrant was divided into nine blocks (45 mm \times 90 mm) and six of them contain only dense arrays of one size pattern (1.5, 3, 5, 10, 30 and 100 μm) in the form of squares or long bars. The additional three blocks of each patterned quadrant contain arrays of various sized openings. Contact printing was used to transfer the patterns to photoresist, and various sized mesa or trench sizes could be obtained, depending on whether positive or negative photoresist was used.

B. MBE GROWTH PROCEDURES

MBE growths were performed in either a Perkin-Elmer 425B or a Riber 2300. Growth on Si substrates was preceded by a 975°C/5-min anneal to desorb the protective oxide grown during chemical etching. Substrate temperature was then lowered and a two-step growth sequence was initiated for GaAs growth. The first growth stage involved deposition of a 120-nm (0.4- $\mu\text{m/hr}$) GaAs layer at 450°C, and the second step consisted of growing GaAs at 525°C at a growth rate of 1 $\mu\text{m/hr}$. Following buffer layer growth, periodic thermal cycling TSL growth was carried out by ramping the substrate temperature up to 650°C and down to 400°C for 5 to 10 times without growth interruption. Each

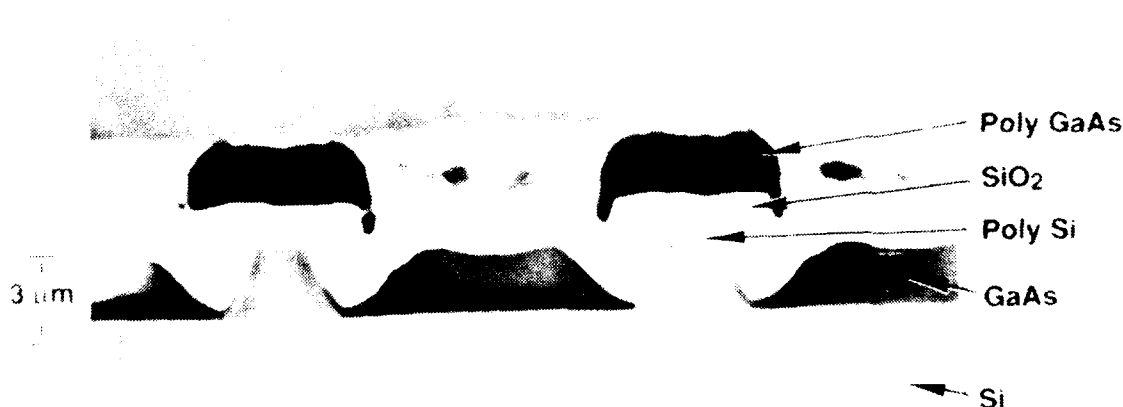


Figure 6
Cross-Sectional Transmission Electron Micrograph of GaAs/Si
Prepared by Cantilever Shadow Masking

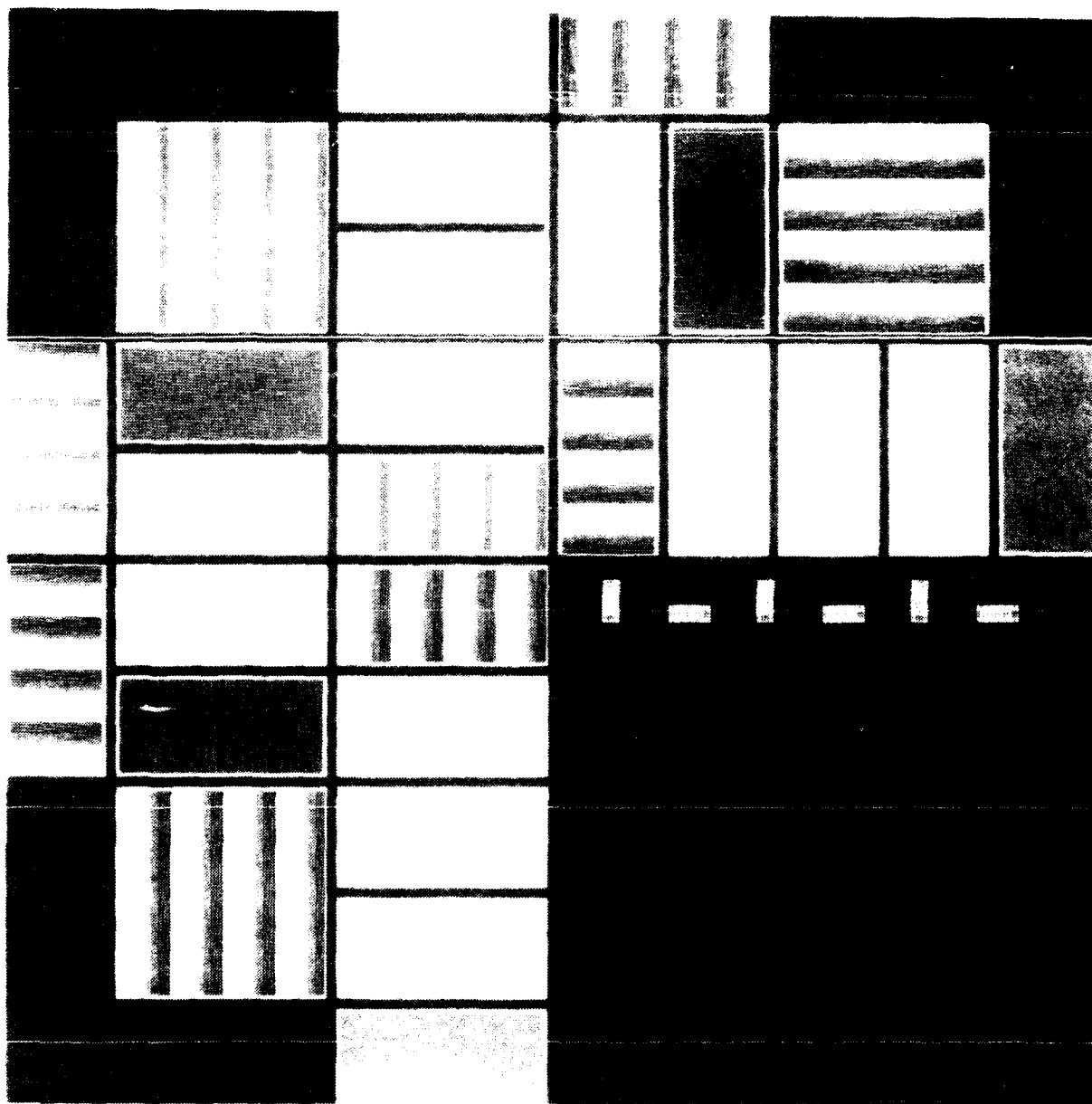


Figure 7
Mask Layout for Selected Area Growth

thermal cycle took 4 min, and GaAs growth at 525°C was resumed after this thermal cycling growth. For the samples where AlGaAs cap anneals were used, a thin $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$ cap layer a few tens of nanometers was grown. The growth was then interrupted and the sample was *in situ* annealed at 850°C for 10 min. Arsenic overpressure was maintained at 1×10^{-5} Torr during this high-temperature AlGaAs cap annealing. GaAs overlayer growth was resumed once the substrate temperature and As overpressure was reduced to normal growth conditions of 525°C and 2×10^{-6} Torr, respectively. Figure 8 shows a schematic growth profile for these procedures. For the samples where strained-layer superlattices were incorporated, five periods of $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ -10-nm/GaAs-10-nm were grown.

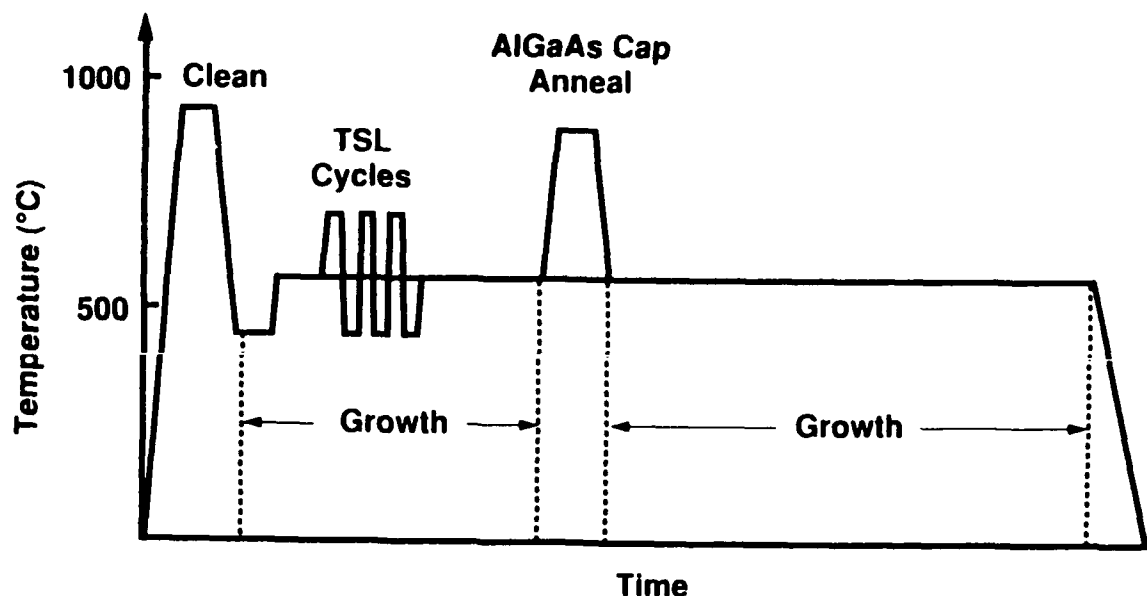


Figure 8
Growth Temperature Profile for the Two-Step GaAs Grown on Si including Thermal-Strained Superlattices and AlGaAs Cap *In Situ* Annealing Processes

Growth on GaAs substrates was preceded by an anneal at 630°C for 10 min under an arsenic overpressure to desorb the native oxides. Growth of $\text{In}_x\text{Ga}_{1-x}\text{As}$ was initiated with a 100-nm GaAs buffer layer to ensure a high-quality heterointerface. The optimum $\text{In}_x\text{Ga}_{1-x}\text{As}$ growth conditions and composition control were obtained through extensive growth system calibration. The $\text{In}_x\text{Ga}_{1-x}\text{As}$ growth temperature ranged between 450 to 580°C, depending on the composition desired. Composition-graded samples were grown by varying substrate temperature and the Ga:In flux ratio. In all cases, strained-layer superlattices were composed of five-periods of $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ -10-nm/GaAs-10-nm.

C. MATERIALS CHARACTERIZATION

Photoluminescence and x-ray rocking curves were used for composition determination for the $\text{In}_x\text{Ga}_{1-x}\text{As}$ /GaAs growth calibrations. Double-crystal x-ray rocking curve line-widths were used to assess the average crystalline quality of blanket GaAs/Si layers. Cross-sectional transmission electron microscopy XTEM and cathodoluminescence CL were used for characterizing the defect structures in the InGaAs/GaAs and GaAs/Si samples. XTEM samples were prepared by low-energy argon-ion milling. A Phillips EM430 transmission electron microscope operating at 300 keV was used for this work. As much as possible, relatively low-magnification/large area microscopy was used to obtain representative defect structures.

SECTION III

THE InGaAs/GaAs SYSTEM

A. HOMOGENEOUS GROWTH

The first group of experiments consisted of the homogeneous (direct) growth of $\text{In}_{0.07}\text{Ga}_{0.93}\text{As}$ and $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ on undercut trench and etched mesa patterned GaAs substrates. Figure 9(a) shows an XTEM micrograph from a sample consisting of the direct growth of $\text{In}_{0.07}\text{Ga}_{0.93}\text{As}$ on a 4- μm -wide GaAs mesa. This composition corresponds to a lattice mismatch of 0.51% with respect to the GaAs substrate. A well resolved misfit dislocation array is observed at the heterointerface and has a spacing of approximately 250 nm. In addition, a number of dislocations are observed within the GaAs pedestal. A similar misfit dislocation structure was also found in the material grown in the trenches between mesas. A large number of trench and mesa regions with widths of up to 100 μm were examined, and no threading dislocations were observed. From these results, we estimate that the threading dislocation density is 10^5 cm^{-2} or lower. Figure 9(b) shows a cathodoluminescence (CL) micrograph from 30- μm and 100- μm -wide squares of this same sample. The linear misfit dislocation density as measured from this micrograph is considerably less than that as measured by XTEM, most likely a result of closely spaced groups of dislocations giving rise to the image contrast rather than individual dislocations.¹¹ This image also demonstrates the near complete absence of threading dislocations.

Although considerable work has been focused on the development of an understanding of the processes by which a heterointerface, such as that shown in Figure 9, acquires misfit dislocations, in most cases these processes are not well understood. The best understood mechanism is the formation of misfit dislocations from the glide of threading dislocations under the influence of the mismatch stress to the heterointerface.^{2,23} However, when the substrate dislocation density is low and/or the lattice mismatch is large, the number of threading dislocations will not be sufficient to generate the observed densities of misfit dislocations. In the experiments described in this work, substrate surface etch-pit densities were lower than $1 \times 10^5 \text{ cm}^{-2}$. This implies that for a 30- $\mu\text{m} \times 30\text{-}\mu\text{m}$ square reduced area growth size, approximately one threading dislocation would be present in this area. Therefore, this mechanism cannot account for the large density of misfit dislocations observed in Figure 9. A substantial fraction of the misfit dislocations, in this case, must be generated from a surface or edge source, most likely heterogeneously. Fitzgerald et al.¹⁰ have arrived at a similar conclusion, with the observation of misfit dislocations that extend from edge to edge of reduced growth area mesas. They attribute the activity of the edges as heterogeneous nucleation sites caused by preferential growth at the edges and faceting.

Another possibility for the generation of misfit dislocations is that they may be caused by dislocation multiplication from the interaction of dislocations as they glide to the interface; i.e., from threading and/or edge nucleated sources. However, this type of process would likely result in a high density of threading dislocations at the epilayer surface, since not all of the dislocation interactions would result in favorable glide dislocations for the misfit accommodation. The absence of a high density of threading dislocations, particularly in the examples shown in Figure 9(a and b) indicates that dislocation interactions were not prevalent in this sample.

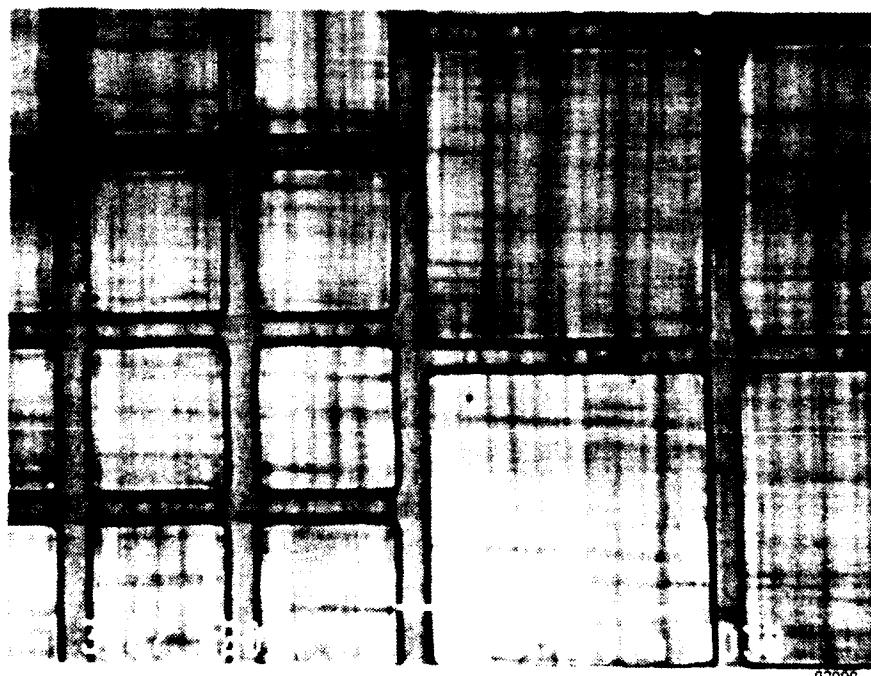
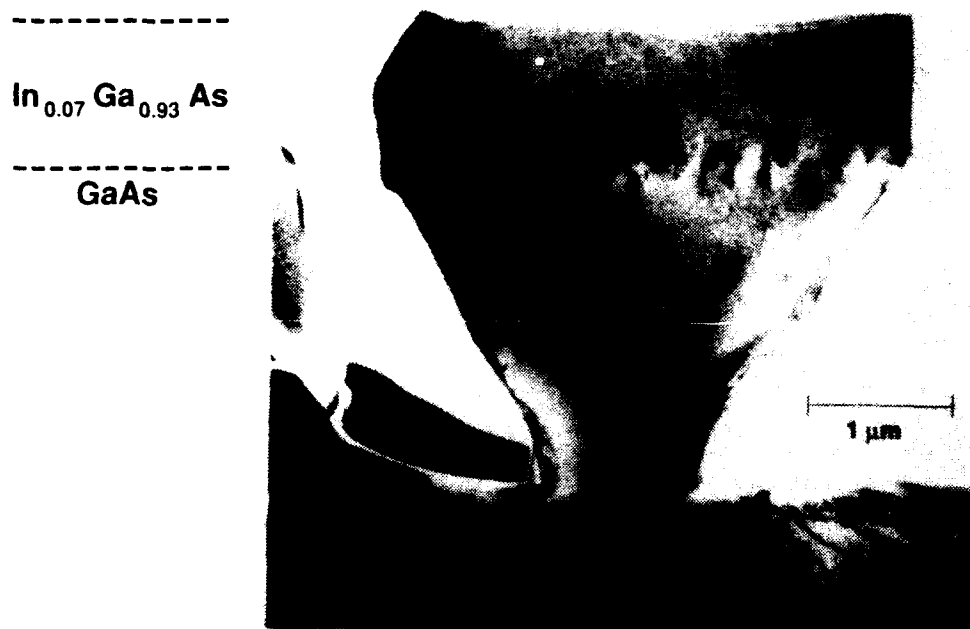


Figure 9
Cross-Sectional Transmission Electron Microscope (XTEM) Micrograph of Direct Growth of $\text{In}_{0.07}\text{Ga}_{0.93}\text{As}$ on 4- μm -Wide GaAs Mesa

Figure 10 shows a micrograph from a sample consisting of the direct growth of $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ within a 10- μm -wide GaAs trench. The lattice mismatch in this case is 1.45% with respect to the GaAs substrate. A very high density of threading dislocations is observed aligned both perpendicular to and at a 45° angle to the substrate surface. The

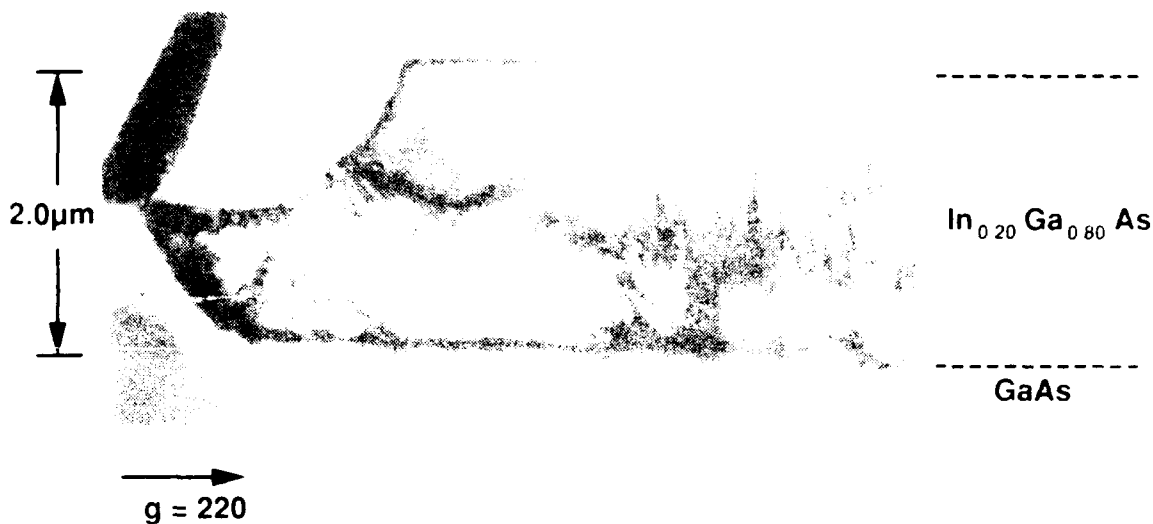
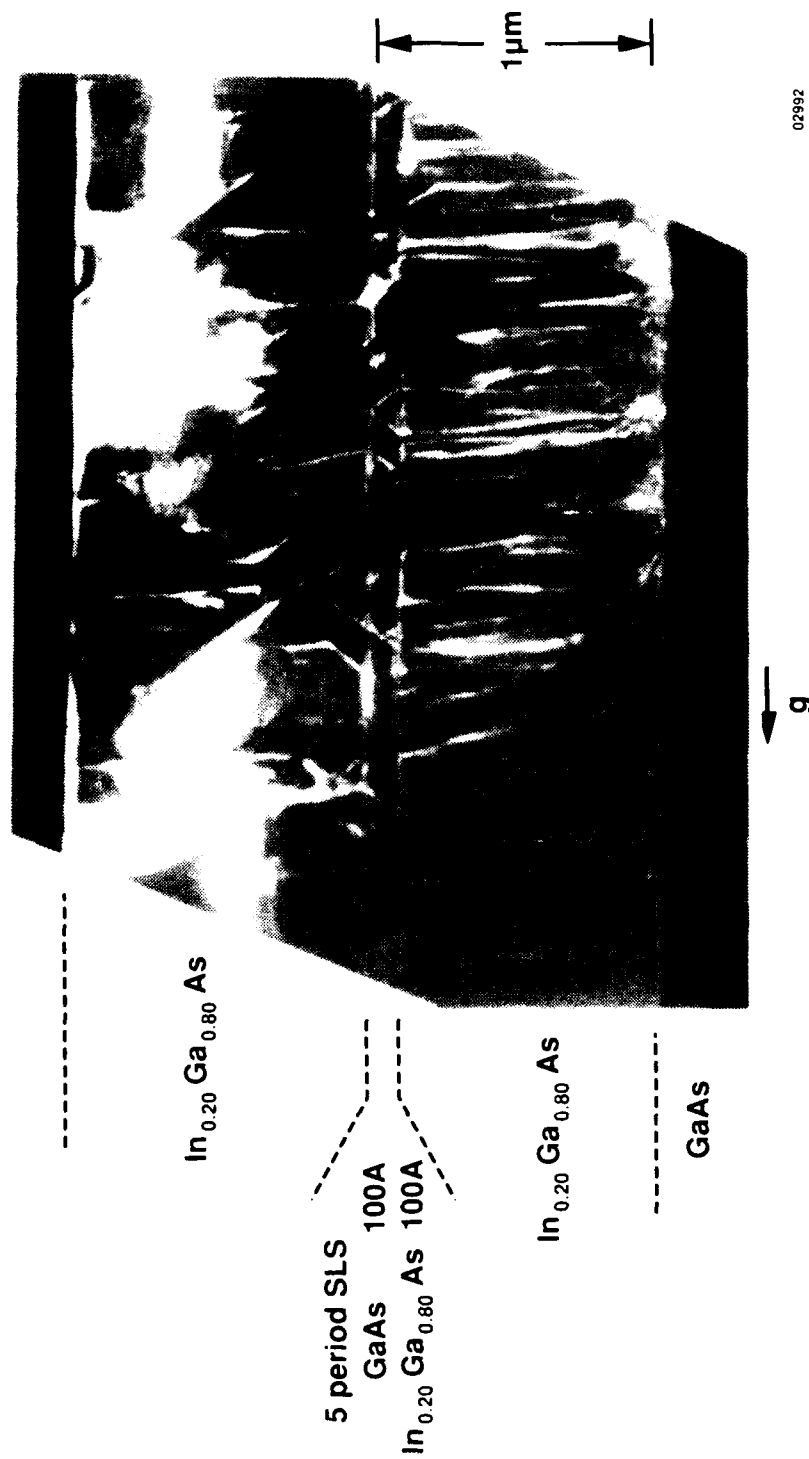


Figure 10
XTEM Micrograph of Direct Growth of $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ in a 10- μm -Wide GaAs Trench

density is somewhat lower near the boundary of the reduced growth area. Material grown on mesas exhibited a similar defect structure. Figure 11 shows a micrograph from a similar sample with the addition of an intermediate five-period $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ -10-nm/GaAs-10-nm strained-layer superlattice (SLS.) The addition of the SLS resulted in a reduction in threading dislocations by about a factor of three. This image shows that the effect of the SLS was the promotion of favorable dislocation interactions over a relatively short range (on the order of 100 nm).

The remarkable difference in defect structure between the $\text{In}_{0.07}\text{Ga}_{0.93}\text{As}/\text{GaAs}$ and the $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}/\text{GaAs}$ sample indicates that serious impediments to efficient misfit accommodation arise during high In composition growth. Three-dimensional (island type) growth or growth in the presence of a large number of surface defects could lead to less efficient misfit accommodation, and is most likely what has occurred for the $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ directly grown on GaAs, as shown in Figures 10 and 11. The high-density of defects that are observed in this material are quite similar to the pyramidal-dislocation tangles (PDTs) observed by Chu et al.²⁴ in $\text{In}_x\text{Ga}_{1-x}\text{As}$ latticed-matched layers grown on indium phosphide. These defects consist of dense dislocation tangles near the interface from which threading dislocations oriented nearly parallel to the growth direction propagate. Chu et al.²⁴ have identified Ga- and P-rich precipitates as the sources for these PDT defects. Three-dimensional island-type growth may promote segregation of the growth species, leading to precipitate formation, and/or it may lead to a highly defective structure during island coalescence. Evidence exists theoretically²⁵ and experimentally²⁶ to suggest that as the In concentration (i.e., strain level) in $\text{In}_x\text{Ga}_{1-x}\text{As}$ increases, the growth mode for MBE-grown $\text{In}_x\text{Ga}_{1-x}\text{As}$ on GaAs changes from two-dimensional to three-dimensional. During three-dimensional growth, as individual islands exceed the critical thickness, separate misfit dislocation arrays would be generated in each island. During



02992

Figure 11
 XTEM Micrograph of Direct Growth of $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ With an Intermediate 5-Period $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}/\text{GaAs}$
 Strained-Layer Superlattice in a 10-μm-Wide GaAs Trench

coalescence of these islands, unless the misfit dislocations are of the proper Burgers vector and are in proper spatial registration from island to island, a large number of threading dislocations would be produced, as shown in Figure 1.

The use of a strained-layer superlattice within a high-defect-density epilayer, such as that obtained with the direct growth of $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$, is found to be of relatively little benefit. The reaction and annihilation of dislocations on a relatively short-length scale is observed; however, for this high a defect density, the SLSs are not effective for driving the dislocations to the edge of the growth areas. Therefore, a growth strategy is required to prevent or lessen the extent of the three-dimensional mode of epilayer growth and the resulting high density of threading dislocations.

B. COMPOSITION-GRADED GROWTH

In an attempt to improve the efficiency of the misfit accommodation process by distributing the misfit dislocations over a finite thickness, as opposed to a single interface, and to prevent the breakdown of the growth interface from two- to three-dimensional, we have employed two composition-grading techniques: step- and linear-composition grading. In this section, the results are presented first for the step-composition-graded growth samples and then for the linear-composition graded samples. A discussion of the combined results is then presented.

1. Reduced Area Growth with Step-Composition Grading

Figure 12 presents an XTEM micrograph from a sample composed of the step-graded compositions $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}/\text{In}_{0.07}\text{Ga}_{0.93}\text{As}$ on a 10- μm -wide GaAs mesa. In addition, two five-period $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ -10-nm/GaAs-10-nm strained-layer superlattices are incorporated at two levels within the $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ layer. A significant reduction in the number of threading dislocations is observed in this case compared to the direct growth as shown in Figures 5 and 6. However, high density defect regions are observed near the growth edges. The SLSs in this sample have effectively bent most of the residual threading dislocations away from the surface toward the epilayer edges, and can be seen piling up at the high-defect-density centers near the edges (arrowed region).

Figure 13 presents an XTEM micrograph from a sample composed of the step-graded compositions $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}/\text{In}_{0.20}\text{Ga}_{0.80}\text{As}/\text{In}_{0.14}\text{Ga}_{0.86}\text{As}/\text{In}_{0.07}\text{Ga}_{0.93}\text{As}$ on a 10- μm -wide GaAs mesa. The right edge of this micrograph shows the actual edge of the reduced growth area. Four distinct interfaces and associated misfit dislocation arrays are observed. Misfit dislocations are observed to be terminated effectively at the epilayer edges and very few threading dislocations were observed propagating to the epilayer surface. The same type of defect structure was observed for the same growth structure inside of cantilever-patterned trenches. The top $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$ layer represents a 1.8% lattice mismatch with respect to the underlying GaAs substrate. As a comparison, Figure 14 shows the typical structure obtained for this same layer sequence on a large area (blanket) region of this sample. From XTEM, regions typically from 20- to 30- μm wide were observed to be relatively free of threading dislocations. However, large dislocation density pile-ups were observed to border these regions, an example of which is delineated by the arrows in Figure 14. These high-density/low-density regions were observed to be randomly distributed through the epilayer composite. The widths of the low-density regions suggest that reduced growth areas with widths of up to 20 to 30 μm should

5 Period SLS $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$
GaAs 100Å
 $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ 100Å
5 Period SLS
GaAs 100Å $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$
 $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ 100Å $\text{In}_{0.7}\text{Ga}_{0.93}\text{As}$



02491

Figure 12
XTEM Micrograph of a Two-Layer Step-Composition-Graded Epilayer on a 10-μm-Wide GaAs Mesa. Note that the upper layer contains two intermediate 5-period $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ strained-layer superlattices. The arrows point to dislocations piled up at a high-density defect center.



02486

Figure 13
 XTEM Micrograph From a Four-Layer Step-Composition-Graded Epilayer on a 10- μm -Wide GaAs Mesa.
 Note that the misfit dislocations are terminated at the edge of the growth area (right side of the micrograph).



02494

Figure 14

XTEM Micrograph From the Same Growth Structure as Figure 18 (but from a Large-Area Blanket Region). The relatively threading-dislocation-free area on the left side of this micrograph extends for about $25\ \mu\text{m}$ to the left, and is bounded by a dislocation pile-up similar to the one on the right side of this micrograph.

effectively have the misfit dislocations terminating at the growth edges, and Figure 15 shows a typical micrograph taken from a 30- μm -wide trench with this same growth structure. Figures 13 through 15 also demonstrate the image-contrast characteristic of phase separation for the composition step $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ and with increased definition for the composition step $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$. Phase separation is not clearly resolved in the $\text{In}_{0.07}\text{Ga}_{0.93}\text{As}$ and $\text{In}_{0.14}\text{Ga}_{0.86}\text{As}$ composition layers.

Attempts were made to extend this step-composition grading technique to higher In compositions. Figure 16 shows an XTEM micrograph from a step-graded growth sequence in a 12- μm -wide trench and is comprised of 7 atomic percent In steps to a top-layer composition of $\text{In}_{0.35}\text{Ga}_{0.65}\text{As}$. It is observed that the step-grading defect density reduction scheme breaks down as the In composition exceeds 21% percent in this case. The density of these threading dislocations was relatively uniform for material grown on mesas and in trenches, and showed no variation with growth area size. Figure 17 shows higher magnification micrographs for a group of threading dislocations in the 28% and 35% In composition layers. The three dislocations delineated by arrows in Figure 17(a) are out of contrast in Figure 17(b), which corresponds to the [004] two-beam diffraction condition. This indicates that the Burgers vectors for these dislocations are parallel to the substrate surface. Also, these dislocations are aligned roughly in the [001] direction, which implies that they are not on a $\langle 111 \rangle$ type habit plane. Attempts to step-grade the composition to higher In composition levels resulted in considerably higher defect densities.

2. Reduced-Area Growth with Linear-Composition Grading

As a comparison to step-composition graded growth, linear-composition grading was employed. Figure 18 shows an XTEM micrograph from a sample in which the In composition was graded smoothly from 0 to 25%. In this case, the growth was in a 10- μm -wide cantilever-patterned trench. The misfit dislocations in this sample are distributed through a thickness of approximately 1.5 μm and are terminated effectively at the epilayer edge (right side of the micrograph). This micrograph also demonstrates the smooth surface morphology that can be obtained. Similar to the case when step-composition grading is used, material grown with the same structure as in Figure 18 in blanket areas exhibited regions 20- to 30- μm wide relatively free of threading dislocations bordered by high-density-dislocation pile-ups. The phase-separation contrast is considerably less developed in the linearly-composition graded epilayers, compared to the step-composition graded layers (compare the 25% In composition regions in Figures 13 and 15).

Figure 19 shows an XTEM micrograph from material grown within a 10- μm cantilever-patterned trench in which the In composition was linearly graded from 0 to 53% In. The lattice mismatch in this case is 3.8% for the material within 0.7 μm to the surface, compared to the GaAs substrate, and this mismatch is accommodated through a thickness of approximately 1.5 μm . Again, it is observed that this defect density reduction scheme is less effective for the higher In compositions; however, the defect density is considerably lower than that when step-composition grading is used. Similar to the case in Figure 18, the phase-separation contrast is not as obvious as with the use of step-composition grading.



02497

Figure 15
XTEM Micrograph From the Same Growth Structure as
Figures 8 and 9 in a 30- μm -Wide Trench

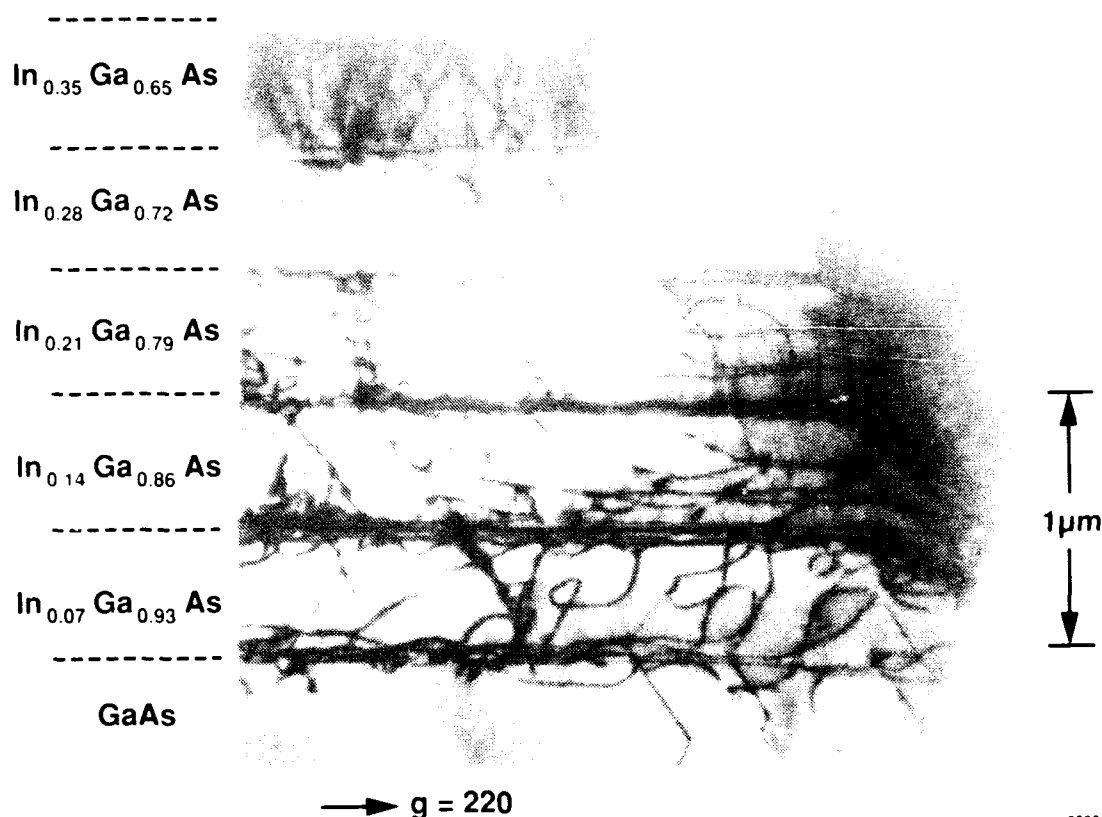


Figure 16
XTEM Micrograph From a Five-Layer Step-Composition-Graded
Epilayer in a 10-μm-Wide GaAs Trench

3. Discussions of Composition Graded Growth Results

We have observed a considerable improvement in the quality of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ with the use of both step- and linear-composition grading. Comparing the micrographs in Figures 10 and 12, the insertion of the $\text{In}_{0.07}\text{Ga}_{0.93}\text{As}$ layer between the GaAs substrate and the $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ layer had a tremendous effect on the resulting number of threading dislocations. The reason for the presence of high-defect-density clusters near the edges of the layer in Figure 12 is not clear, but it is most likely caused by a poor cleanup of the surface prior to growth. The SLSs are also observed to be more effective than in the case discussed above. Since the number of threading dislocations is relatively small, the dislocations, which are pulled into the SLS, are able to propagate considerable distances toward the epilayer edges. In the case shown in Figure 12, they have run into the high-defect-density regions and have been pinned.

Comparing the step- and linear-composition-graded reduced-area growth samples (Figures 13 and 18), it is clear that both of these techniques are effective for spatially separating misfit dislocations in a direction perpendicular to the original interface, and facilitating the termination of these dislocations at the reduced-area growth edges. However, it is also interesting to note that the contrast associated with phase separation in the

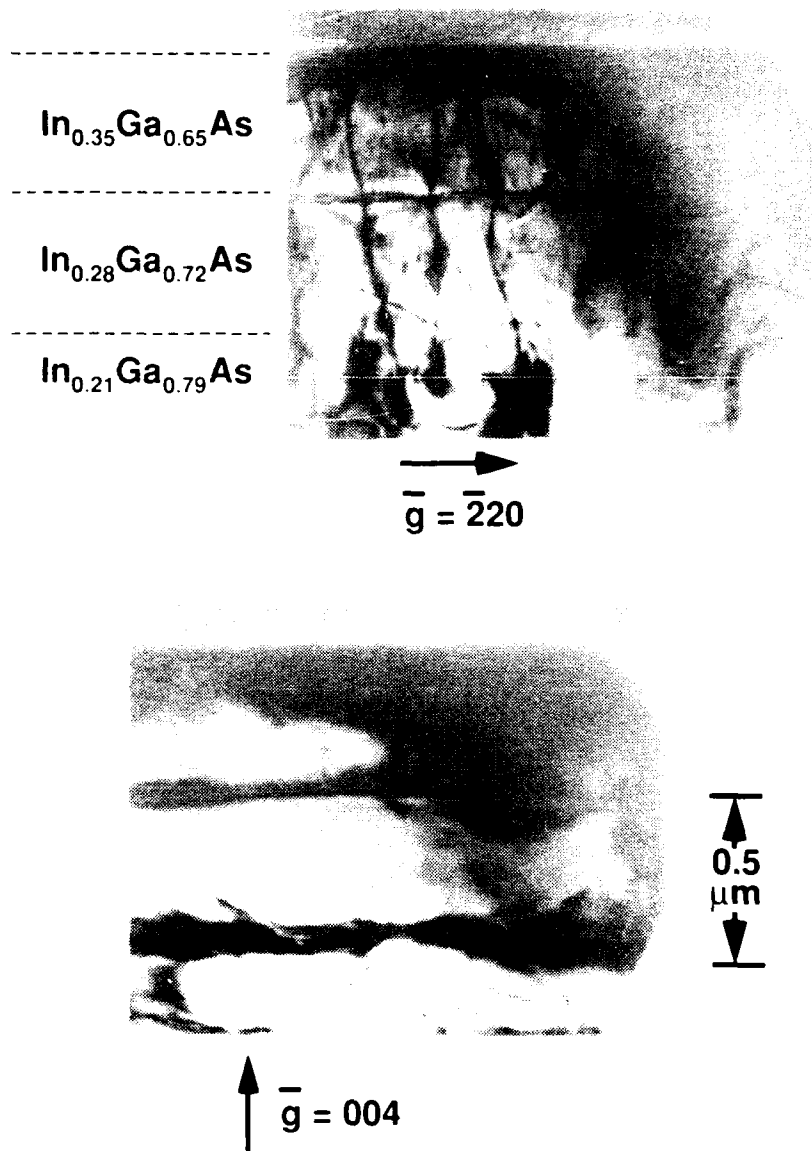


Figure 17
XTEM Micrograph of Threading Dislocations in the Top Two Layers for the Same Growth Structure as in Figure 20. (a) The dislocations are in contrast for \vec{g} parallel to the interfaces, and (b) they are out of contrast for \vec{g} perpendicular to the interfaces.

top $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$ layer is somewhat less developed in the linearly graded sample compared to the step-graded sample. This may be related to the growth mechanism, such that the gradual composition change that occurs with the linear grading better preserves the two-dimensional growth nature.

The usefulness of reduced-growth areas with the composition-grading techniques is exemplified by the comparison of the defect structures observed in reduced-growth-area regions with that of blanket regions. Figure 14 shows that while low-defect-density regions can be found in the blanket regions, they are generally bounded by regions where dislocations have piled up to form very high-density threading-dislocation centers. The



Figure 18
XTEM Micrograph From a Linear-Composition-Graded Epilayer to In_{0.25}Ga_{0.75}As
in a 10-μm-Wide GaAs Trench. Note that the dislocations terminate at the epilayer
edge on the right side of the micrograph.

locations of these high-defect-density regions are not uniform and are not predictable, and therefore, from the standpoint of device fabrication, would lead to high yield losses. The formation of these high-defect-density regions in blanket areas can be rationalized by considering Figure 20. Blanket areas in this case refer to areas of dimension $L \gg l$, where l is the mean free path of the dislocations gliding into the interface from surface half-loop nuclei. Figure 20(a) shows the initial stage of the misfit accommodation process where a small number of half-loops have been formed and are propagating in the epilayer to the interface. In Figure 20(b), the dislocation segments labeled 1, 2, and 3 in Figure 20(a) have impinged upon one another and in this case have not reacted to annihilate or to produce a resultant dislocation segment. Rather they have piled-up to form a threading dislocation cluster. As growth proceeds, and additional misfit dislocations are nucleated, provided favorable dislocation interactions do not occur when they run into the threading dislocation cluster, they too will pile up to enlarge the cluster, as shown in Figure 20(c). Thereby, the defect cluster will grow until all of the misfit dislocations have been generated. These dislocation pile-ups would closely resemble the pile-up observed in Figure 14. Reducing the growth area to a dimension less than the mean free path length for the dislocations should prevent these types of threading dislocation clusters.

Limitations of reduced growth area for the prevention of dislocation interactions can be rationalized in terms of the lifetime of a misfit-forming glide dislocation, i.e., the time required for the dislocation to propagate to the edge of the growth area once generated. Consider the quarter-loop dislocation formation mechanism depicted in Figure 21. For this illustration, assume that all of the misfit-accommodating dislocations are formed



1 μm

$\bar{g} = \bar{2}20$

Figure 19
XTEM Micrograph From a Linear-Composition Graded Epilayer to
 $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ in a 10- μm -Wide GaAs Trench

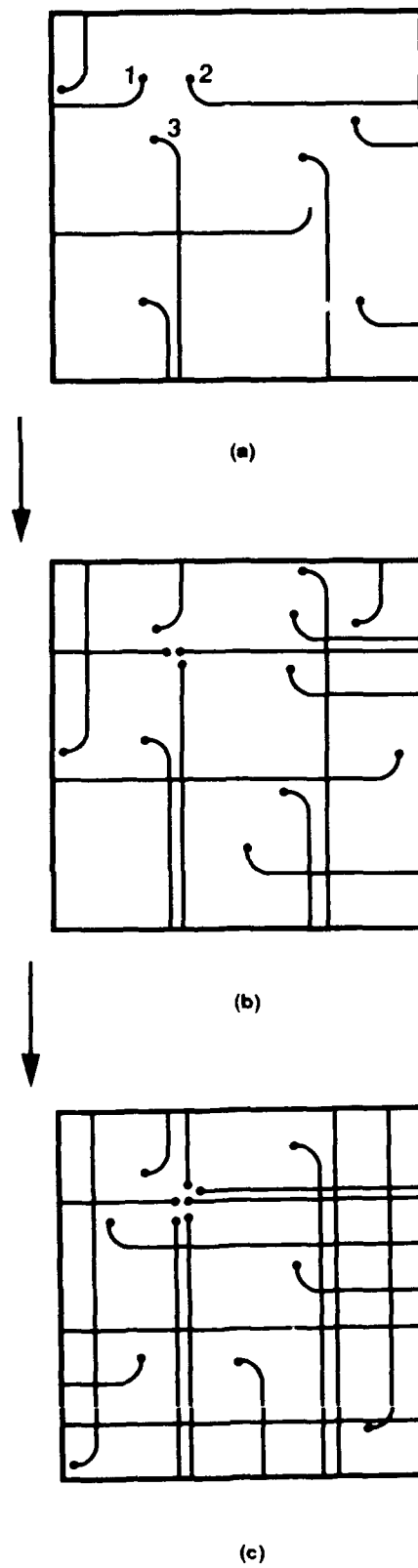
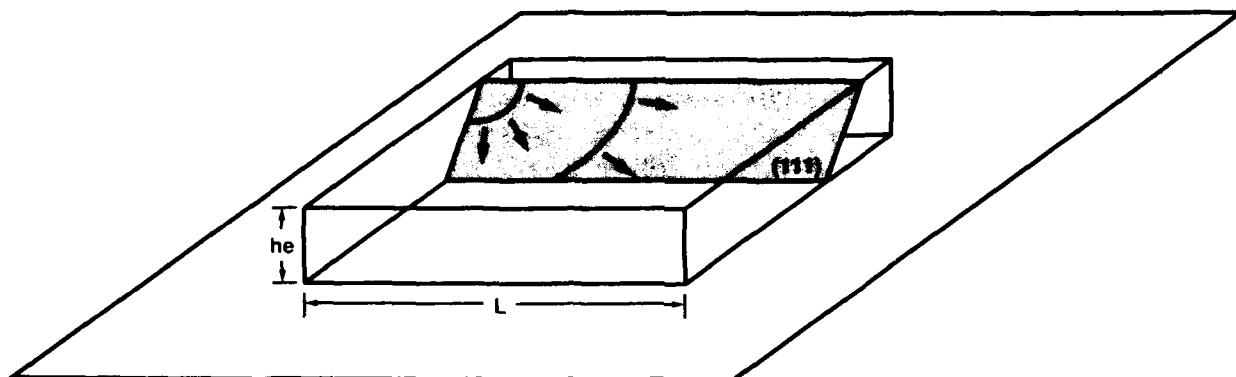


Figure 20
Schematic Description for the Formation of High-Density Dislocation Pile-Up Centers in Large-Area Lattice-Mismatched Epilayers (i.e., $l \ll L$)



03087

Figure 21
Edge Nucleation of Glide Dislocation Quarter-Loops for Misfit Accommodation

from glide dislocations that are nucleated at a constant rate from edge heterogeneous sources in the form of quarter-loops, and that the number of dislocations generated in the area from the edge sources is directly proportional to the length of the edges of the growth areas. The lifetime of the dislocations generated in the small area of width L in Figure 22(a) is given by $\tau = L/v$ where v is the glide velocity of the dislocations. Assume that the dislocation nucleation rate is such that for each dislocation, which is terminated at the edge of the growth area in time τ , another dislocation is nucleated at the epilayer edge. For a larger growth area of width nL [Figure 22(b)] the lifetime of the gliding dislocations is given by $n\tau$. If the dislocation nucleation rate is the same as that for the smaller area, additional dislocations are generated before the original dislocations traverse the growth area. As such, at steady state, the density of gliding dislocations in the small and large areas are the same. Now, consider the mean free path for a dislocation gliding to a heterointerface that can be approximated as $l = 1/h\rho$, where h is the epilayer thickness and ρ is the glide dislocation density.¹⁷ Since the steady state gliding dislocation density is independent of growth area, the mean free paths for the dislocations in Figures 22(a) and 22(b) are the same. Therefore, to prevent dislocation interactions during the misfit-accommodation process, a growth area of width $nL \leq l$ is required.

The implication of the previous discussion is that the growth area size for which dislocation interactions are unlikely depends on the nucleation rate of the dislocations. If the rate of nucleation is slow relative to the dislocation lifetime τ , the growth area size for which $L \leq l$ will be larger. Since the dislocation nucleation rate is dependent on the growth rate, this implies that slowing the growth rate will facilitate the use of larger growth areas. In addition, composition grading should result in larger growth areas free of dislocation interactions, since the nucleation rate can be modified by grading the lattice misfit with growth thickness/time.

Another possible mechanism that would lead to a dislocation pile-up, and that would not be improved with a reduction in growth size, is a defective region initiated at the growth interface because of surface damage or a poor pregrowth cleanup. This type of situation may account for the dislocation pile-ups observed in Figure 12.

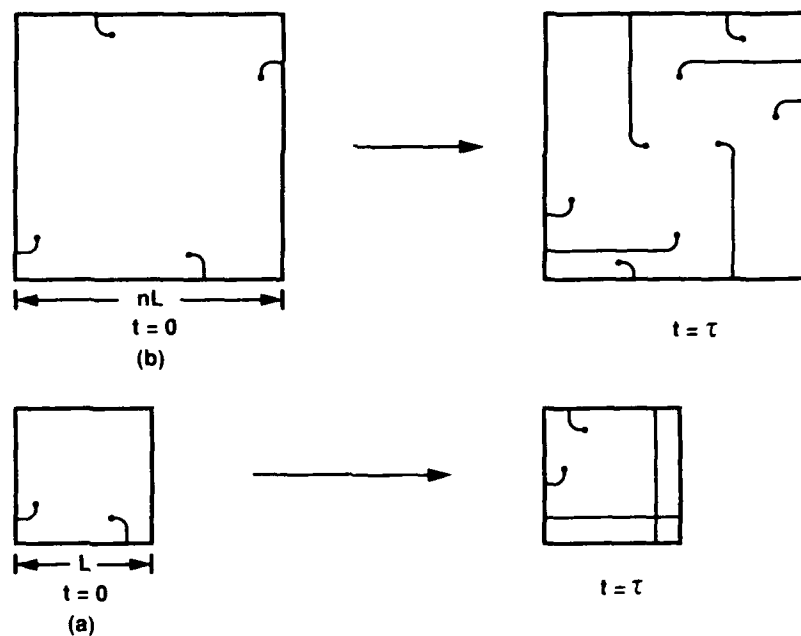


Figure 22
The Effect of Reduced Area Growth Size on Dislocation Dynamics

Step-grading the $\text{In}_x\text{Ga}_{1-x}\text{As}$ composition beyond $x = 0.25$ generally resulted in poor-quality epilayers, as shown in Figure 16. This is most likely a result of a transition to a three-dimensional mode of growth with increased In composition, as described by Chen et al.²⁶ The phase separation that is observed may facilitate or may also be related to the roughening of the growth interface. The roughened growth interface would likely facilitate the heterogeneous activation of additional misfit dislocation nuclei and, therefore, cause a greater number of dislocation interactions. The presence of the large number of threading dislocations, which have Burgers vectors parallel to the growth surface, as shown in Figure 17, are likely formed by the interaction of two glissile 60° dislocations with Burgers vectors in the same $\{111\}$ glide plane, as described by Fitzgerald et al.²⁷ The line orientation of these dislocations parallel to the growth direction (i.e., not on a $\{111\}$ type plane) suggest that they are formed close to the heterointerface and then propagate during crystal growth. This growth orientation can be rationalized in terms of energy considerations and the atomic mechanism of crystal growth.²⁸ These dislocations are sessile under the influence of the biaxial misfit stress and can act as barriers to other gliding dislocations.²⁷ This effect is enhanced by the fact that the line orientation of these dislocations in the $[001]$ growth direction threads through a large number of $\{111\}$ planes. As such, gliding 60° dislocations, which propagate within a volume on the order of the square of the epilayer thickness surrounding these threading dislocations, will run into these threading dislocations. Therefore, the formation of this type of threading dislocation must be prevented for there to be a significant reduction in defect density. Prevention of the formation of these types of dislocations should be facilitated by a reduction of growth area to less than the mean free path dimension of the gliding dislocations and by maintaining the two-dimensional mode of crystal growth.

The use of linear-composition grading for higher In compositions appears to be substantially better than for step-composition grading, as can be seen by comparing Figures 16 and 19. The reason for this difference is not clear, but may be related to a less extensive roughening of the growth interface. The less well-developed phase-separation contrast in the linear-composition-graded layers also suggests a difference in growth mechanism. The result shown in Figure 19 suggests that linear-composition grading shows the most promise for large latticed-mismatched heteroepitaxy in reduced areas. Optimization of the growth properties such as growth temperature, growth rate, and composition-grading rate warrant further investigation. In addition, Chen et al.²⁶ have shown that migration-enhanced epitaxy (MEE) can be used to maintain a two-dimensional growth mode for high-strain values of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$.

SECTION IV

THE GaAs/Si SYSTEM

The GaAs/Si system has a considerable disadvantage compared to the $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ system described in the previous section, as intermediate alloy composition grading is less convenient. Lattice mismatch is accommodated at a single interface. The elimination of the composition variation degree-of-freedom limits the dislocation-reduction strategies for both large- and reduced-area growth to annealing and strained-layer superlattice dislocation filtering.

As discussed in the previous section, dislocation filtering techniques will only be useful when the defect density is sufficiently low such that the dislocations can be bent to the edge of the growth area without interactions with other dislocations. On the other hand, annealing techniques are expected to be useful only when the dislocation density is high, i.e., when the dislocations are spaced closely enough that their strain fields strongly interact. With this in mind, we used a two-step approach. We first investigated the use of *in situ* annealing techniques to lower defect density. Homoepitaxial growth *in situ* annealing techniques with other materials systems suggest that this limit is in the 10^5 to 10^7 cm^{-2} range.²⁸ We subsequently incorporated dislocation filtering techniques after *in situ* annealing.

The discussions of our GaAs/Si results are organized as follows: dislocation reduction techniques previously developed for large area epilayers, various types of reduced area growth strategies that we have used and the problems associated with these techniques, and the use of the cantilever shadow masked growth technique with various combinations of *in situ* annealing and dislocation filtering.

A. LARGE-AREA (BLANKET) GROWTH

Considerable work at Texas Instruments has been focused on the reduction in defect density of large-area (blanket) grown GaAs/Si. Several strategies have been developed that result in defect densities of 10^{-7} cm^2 or lower. These strategies include various growth initiation methods, *in situ* annealing techniques,²⁹ and postgrowth annealing. An understanding of the mechanisms that lead to the observed improvements in epilayer quality and the limitations to their effectiveness provides a basis for the study of the effects of reduced-area growth.

Recently, Kao et al.²⁹ have developed *in situ* annealing techniques that result in the highest quality large-area GaAs/Si epilayers reported to date. Figure 8 shows the growth sequence used to produce these results. Figure 23 presents an XTEM micrograph from their work. It is observed that the *in situ* annealing techniques promote dislocation interactions on a relatively short-length scale; i.e., threading dislocations, which are initially closely spaced, are observed to react to annihilate or to form a single resultant dislocation. The intrinsic limit for the effectiveness of *in situ* annealing techniques is related to the decay in magnitude of the dislocation interaction stress fields with dislocation separation distances and for GaAs/Si this limit appears to occur at a dislocation density in the low 10^6 cm^{-2} range. A similar limit is obtained for the homoepitaxial growth of III-V materials on high dislocation density substrates in which intermittent growth procedures are employed.^{28,30} Therefore, for further improvement in epilayer

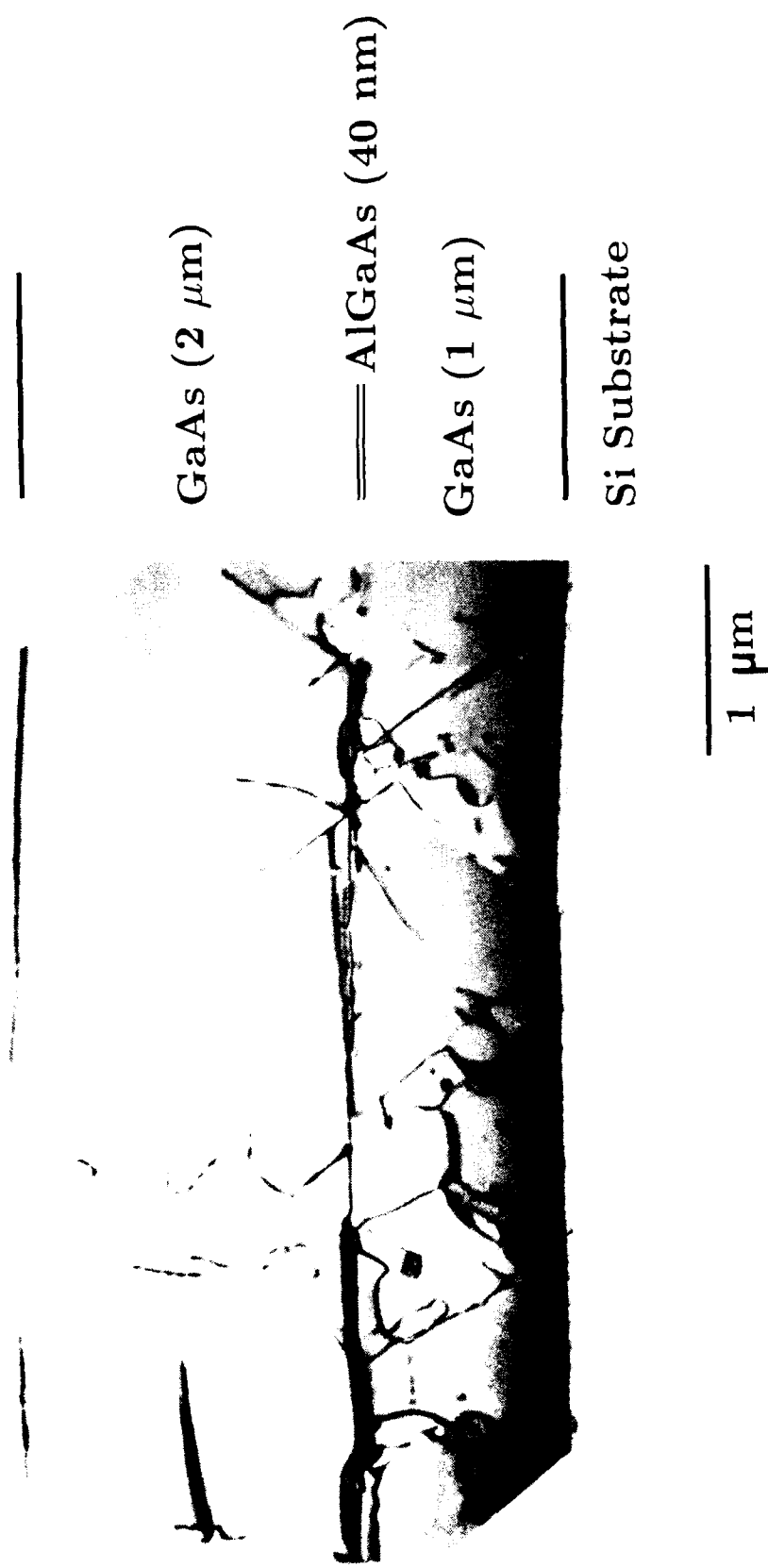


Figure 23
 Cross-Sectional TEM Micrograph of GaAs/Si Prepared Using Thermal Superlattice Layers and Followed by an AlGaAs Cap Anneal

quality, a method of moving dislocations is required whereby dislocation interactions are promoted or the dislocations are driven to the edge of the growth area.

The use of strained-layer superlattice *dislocation filtering* is one means for moving dislocations. However, as discussed in the previous section, the use of a misfit strain to move dislocations in an epitaxial layer can lead to both favorable dislocation interactions or to dislocation multiplication. As such, simply promoting dislocation interactions is not a feasible method for completely eliminating threading dislocations. A more promising approach is to drive the dislocations out of the epilayer at the epilayer edges. Similar to the reasoning described in the last section, the use of reduced growth areas is the most likely means of accomplishing this goal.

B. REDUCED-AREA GROWTH

Our initial studies of reduced-area growth of GaAs/Si were performed by growing over oxide-patterned Si substrates. As such, deposition occurred both inside of the windows in the silicon oxide as well as on top of the oxide-patterning layer. Figure 24 shows an XTEM cross-sectional micrograph from one of these growth structures. It is observed that a large density of twins is generated at the polycrystal/single-crystal interface. These twins extend into the single-crystal GaAs region a distance comparable to the growth thickness. The defect density within the single-crystal regions is comparable to that obtained from blanket-grown GaAs/Si. The twins that propagate into the single-crystal GaAs region are not desirable since they inhibit the movement of dislocations out of the reduced growth area regions if strained-layer superlattices are used. Therefore, our next approach was to try and eliminate the polycrystalline/single-crystal interfaces by growing inside of etched Si trenches and on top of etch-defined Si mesas.

Figure 25 shows a cross-sectional SEM view of the growth structure obtained for a sample in which GaAs was grown inside an etch-defined trench in Si. Figure 26(a and b) shows a bird's eye view of this same structure and an XTEM micrograph from the trench edge region, respectively. The GaAs epilayer is observed to grow conformally to the patterned substrate structure. A large density of defects is observed to be generated at the Si sidewall, most likely caused by the variation in growth orientation along the sidewall. Similar to the situation described above, attempts to use dislocation filtering techniques with this type of structure would not be expected to be successful since the high density regions could block the movement of dislocations or, more likely, could act as a source of dislocations.

Figure 27(a) shows an SEM cross-sectional micrograph for a sample in which GaAs was grown on top of etch-defined Si mesas. The growth morphology exhibits well-developed facets near the mesa edges, and the complete elimination of the original (001) growth front. The schematic diagram in Figure 27(b) shows that facets are composed of {111} and {310} surfaces. Considerable sidewall growth is also observed in this micrograph. Figure 28 presents an XTEM micrograph from this same sample. A high density of twins is observed in a direction perpendicular to the {111} growth facets and in the material grown on the sidewalls. The defect density in the central regions of the material grown on wider mesa structures is comparable to that obtained from blanket area growths, and rises considerably as the growth edges are approached. Use of this type of growth structure with dislocation-bending techniques is not likely to be of value.



Si SUBSTRATE

Figure 24
Cross-Sectional TEM Micrograph of the Transition From Single-Crystal
to Polycrystalline Growth in Patterned GaAs-on-Si

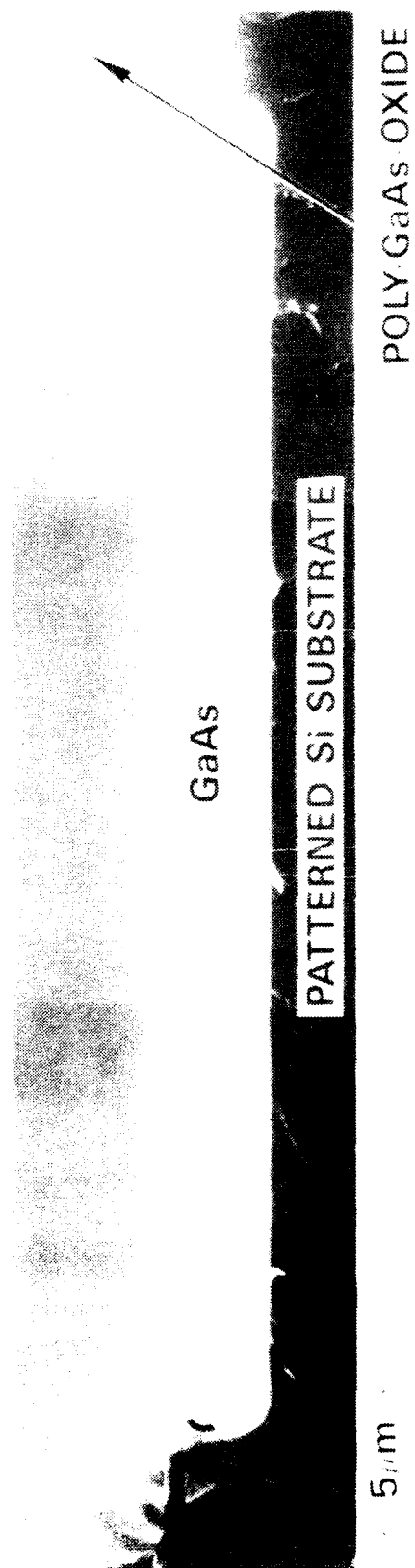


Figure 25
SEM Micrograph of GaAs Grown in a 50- μ m-wide Si Trench

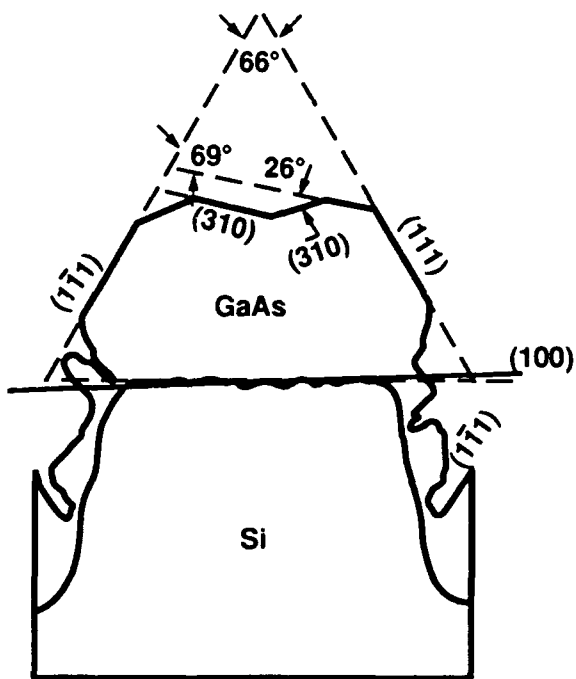


(a) SEM Micrograph of the Patterned GaAs Region



(b) Cross-Sectional TEM of the Trench Sidewall

Figure 26
Cross-Sectional Micrographs of GaAs Grown Over Etch-Defined Si Trenches



00566

Figure 27
(a) XTEM Micrograph of GaAs Grown on 3- μm -wide Si Mesa,
(b) Tracing of This Micrograph



Figure 28
Defect Structure of As-Grown GaAs at the Sidewall of a 100- μ m-wide Si Mesa

What emerges from the above studies is that a reduced-area-growth method is required in which polycrystalline/single-crystal interfaces are avoided, sidewall growth interactions are avoided, and that results in preservation of the (001) growth interface. We found that the use of the cantilever-shadow-masked growth structure is effective for realizing these objectives, and the remainder of the reduced-area-growth experiments to be described were conducted using this technique. Figure 29 shows an SEM micrograph with various sized cantilever-patterned GaAs/Si islands. In this case, the cantilever oxide layer has been removed to show that the GaAs islands are well isolated from the Si sidewalls. Also, this micrograph shows that reduced-area-growth widths as small as 5 μ m can be produced.

Figure 30 shows an XTEM micrograph from a sample consisting of GaAs inside a 10- μ m-wide cantilever-patterned Si trench grown using the two-step growth initiation method. The defect density in the central region of this epilayer is comparable to that obtained from blanket area regions. There is a slight improvement in the regions approximately 2 to 3 μ m from the reduced-area growth edges. This phenomenon was observed for a large number of the samples that we examined and the extent of the reduced-defect-density zone did not seem to be affected by growth-area size. Thus, using the two-step growth method, no significant improvement in defect density is obtained

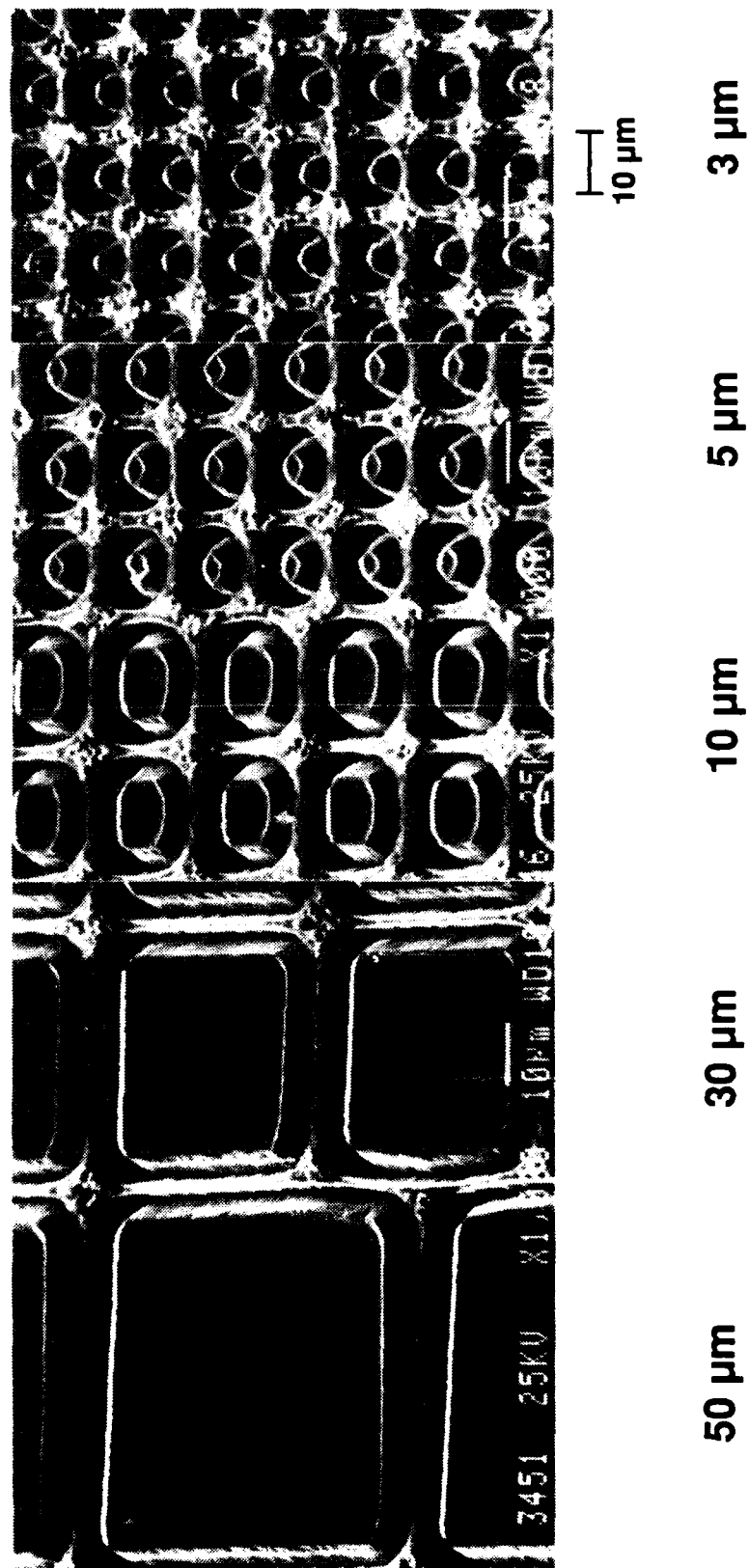


Figure 29
Various Sized Cantilever Mask Patterned GaAs/Si Structure
 Note that the cantilever mask structure has been removed.



Figure 30
XTEM Micrograph From a GaAs Epilayer Grown by the Two-Step Method in a 10-μm-wide
Cantilever Shadow Mask Patterned Si Trench

with reduced-area growth. The slightly lower density observed near the growth edges may be a result of the lessening of the thermal expansion mismatch stresses near the growth edges. These results are consistent with our premise that the benefit of reduced-area growth for defect-density reduction in this materials system may result from improved dislocation filtering effectiveness rather than from an improvement in lattice misfit accommodation process.

To test this idea, we have incorporated strained-layer superlattices after initiating growth by the two-step method. Figure 31 shows an XTEM micrograph from an epilayer in a 10- μm -wide trench. In this case, two 5-period $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ -10-nm/GaAs-10-nm strained-layer superlattices were inserted at 1 and 2 μm from the GaAs/Si interface. Similar to the sample shown in Figure 30, a reduction in defect density is observed only near the epilayer edges. The strained-layer superlattices were only marginally effective for reducing the defect density. The original threading defect density prior to initiation of the strained-layer superlattices is clearly too high for the effective bending of dislocations to epilayer edges. Rather, a large number of interactions have occurred that resulted in a small number of dislocation annihilation reactions. This same situation is observed in the $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ /GaAs sample containing a strained-layer superlattice, as shown in Figure 11. Figure 32 shows the same growth structure inside a 5- μm -wide trench. In this case defect density is lowered considerably. The width of this sample is comparable to the combined reduced defect-density regions near the two edges of the wider stripe shown in Figure 31.

The use of additional strained-layer superlattices in the larger growth-area regions will likely lead to gradually reduced densities of threading dislocation. However, this approach is not particularly attractive since considerably thicker epilayers would be required. A better approach would be to use *in situ* annealing techniques to reduce the defect densities to a level where strained-layer superlattices might have a chance of driving the dislocation to the periphery of the growth areas, i.e., to a density less than $\sim 5 \times 10^7 \text{ cm}^{-2}$. Figure 33 shows an XTEM micrograph from a GaAs epilayer grown inside



Figure 31
XTEM Micrograph From a GaAs Epilayer Containing Two 5-Period SLs inside
a 10- μm -wide Cantilever Patterned Si Trench



Figure 32
XTEM of the Same Growth Structure as Shown in Figure 31 (But in a 5-μm-wide Trench)



Figure 33
XTEM Micrograph From a Portion of a GaAs Epilayer Containing Two AlGaAs Cap Layers Inside a 10-μm-wide Cantilever Patterned Si Trench

of a 10-μm-wide Si trench. In this case, a thermal-strain superlattice (TSL) and two AlGaAs cap anneal cycles were incorporated in the growth sequence. This micrograph demonstrates that *in situ* annealing techniques were extremely effective for promoting short-range defect-annihilation reactions. After examining a large number of growth areas, we estimate that a defect density of less than $5 \times 10^7 \text{ cm}^{-2}$ is obtained, which is comparable to large-area growths incorporating these *in situ* annealing techniques. At this level strained-layer superlattices may be effective for reducing the defect density further.

The next experiment that we performed consisted of the insertion of three AlGaAs cap anneal cycles at 1- μm growth intervals followed by a five-period SLS. Figure 34 shows an XTEM micrograph from this sample from a region within a 10- μm -wide trench. The thickness of this growth structure has exceeded the depth of the trench. As such, the sidewalls of the GaAs layer that protruded through the shadow mask became exposed to the growth constituent beams during MBE growth and resulted in the faceted structure at the epilayer edges. It is apparent that the first AlGaAs cap anneal was the most effective, and virtually no improvement is obtained for the third one. Also, most of the dislocations which thread through the third AlGaAs cap layer also thread through the SLS without being deflected into the interfaces. Figure 35 shows a plan view TEM micrograph from a 5 μm -wide stripe from this sample. This TEM sample was obtained by thinning from the substrate side of the structure. From this sample we obtain a threading dislocation density on the order of $1 \times 10^7 \text{ cm}^{-2}$. Figure 36 shows a series of cathodoluminescence images obtained from various sized areas of this sample. The effect of reduced growth area is clearly seen by comparing the reduced growth areas in Figure 36(b and c) to the blanket growth region in Figure 36(a). Since the defect density is greater than $1 \times 10^6 \text{ cm}^{-2}$, the dark regions in Figure 36(a) are most likely from high-density dislocation clusters formed from pile-ups, as described in Section III. The use of reduced growth areas clearly eliminates these high-density dislocation clusters.

Our final growth structure was comprised of a single AlGaAs cap layer and three five-period SLSs spaced at 0.5- μm intervals in a GaAs epilayer. Figure 37(a and b) shows XTEM micrographs from a region grown within a 10- μm -wide trench. It is observed that most of the dislocations that are deflected into the SLSs do not propagate all the way to the reduced area growth edges. Rather, dislocation interactions are prevalent. Also, similar to the previous sample, a large number of the threading dislocations propagate through the SLS layers without being deflected or bent into the interfaces. The reasons for this behavior warranted additional investigation.

Compare the two dislocations delineated by arrows in Figure 37(a and b). These dislocations exhibit double-image contrast for $g = [\bar{2}20]$ [Figure 37(a)] and are out of contrast for $g = [004]$ [Figure 37(b)]. This is consistent with the assignment of the Burgers vector as $b = \pm 1/2 [\bar{1}10]$. This Burgers vector lies in the interface plane; therefore, the biaxial stress field produced by the SLS would not act on these dislocations in a direction promoting dislocation glide to the interface. Also, it is interesting to note that from the length of the dislocation line images relative to the thin foil thickness ($\leq 1 \mu\text{m}$) these dislocations are not lying on $\{111\}$ type habit planes. This condition also makes these dislocations sessile. The reason for the observed crystallography for these dislocations is most likely related to the atomic growth process and the fact that in anisotropic diamond-cubic or face-centered cubic crystals, edge dislocations have a lower energy on $\{110\}$ planes.³¹ In addition, Beam et al.²⁸ have observed a similar dislocation reorientation in homoepitaxial InP layers grown by liquid phase epitaxy.

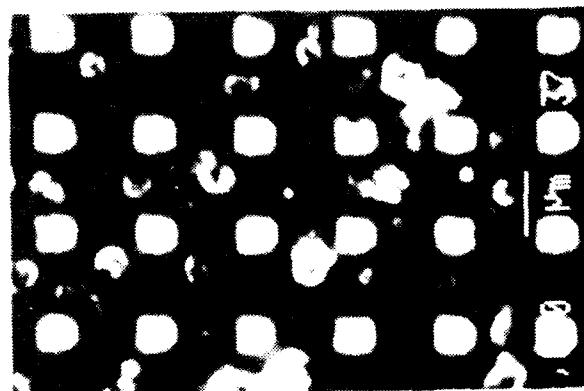
Figure 38(a through f) shows a series of XTEM micrographs under various diffraction conditions for another region of this same growth structure. In this case, consider the dislocations delineated by arrows in Figure 38(a). This group of dislocations exhibits strong image contrast for $g = \pm[\bar{2}20]$ and $g = [\bar{2}\bar{2}\bar{2}]$, double-image contrast for $g = \pm[004]$ and are out of contrast for $g = [\bar{2}20]$. These results are consistent for Burgers vectors of $b = \pm 1/2[101]$ or $b = \pm 1/2 011$. These Burgers vectors are inclined to the (001)



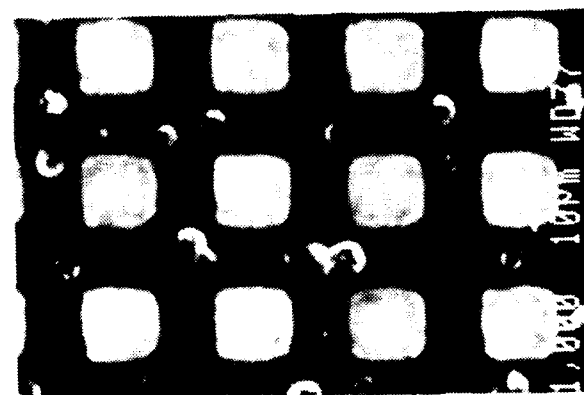
Figure 34
XTEM Micrograph From a GaAs Epilayer Containing Three AlGaAs Cap Layers and a 5-Period SLS in a
10-μm-wide Cantilever Patterned SI Trench



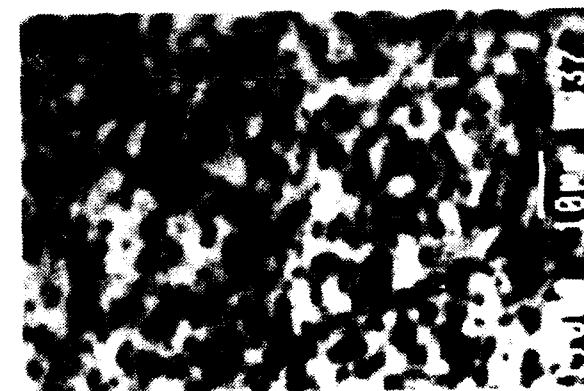
Figure 35
Plan-View TEM Image From a Trench Region of the Same Growth Structure as Shown in Figure 34. The sample was thinned
from the substrate side and exhibits a threading dislocation density of $\sim 1 \times 10^7 \text{ cm}^{-2}$.



5 μ m



10 μ m



**BLANKET GROWTH
AREA**

Figure 36
Cathodoluminescence Images From Various Sized Growth Areas for the Growth Structure Shown in Figure 34



(a)



(b)

Figure 37
XTEM Micrographs From a GaAs Epilayer Containing One AlGaAs Cap Layer and Three 5-Period SLs inside
a 10- μ m-wide Cantilever Patterned Si Trench

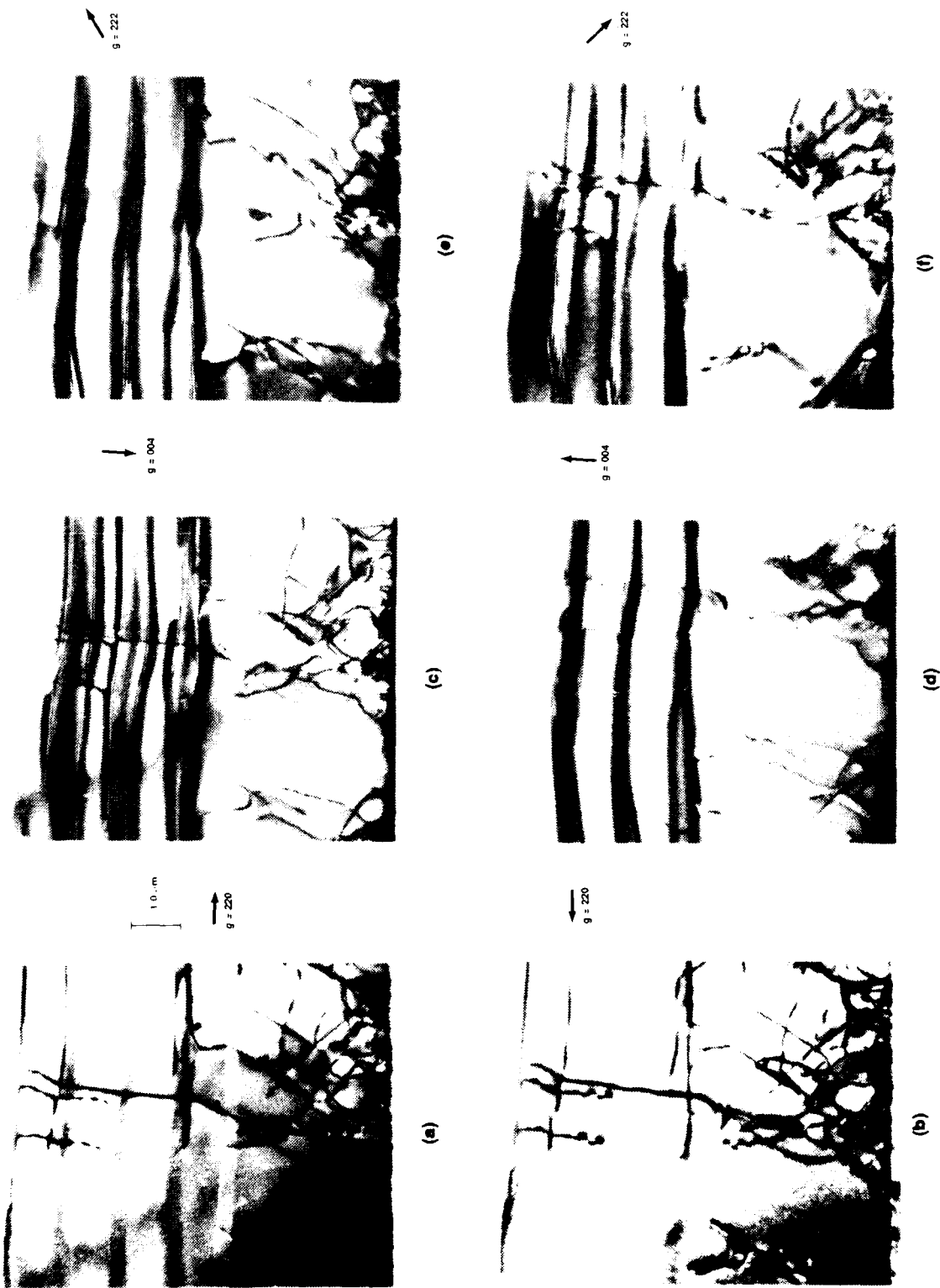
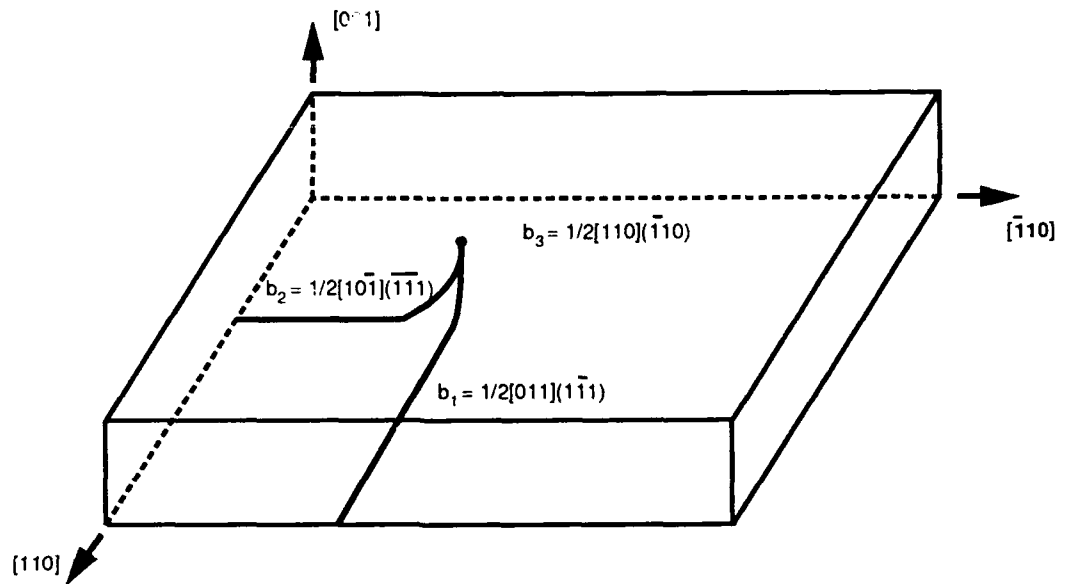


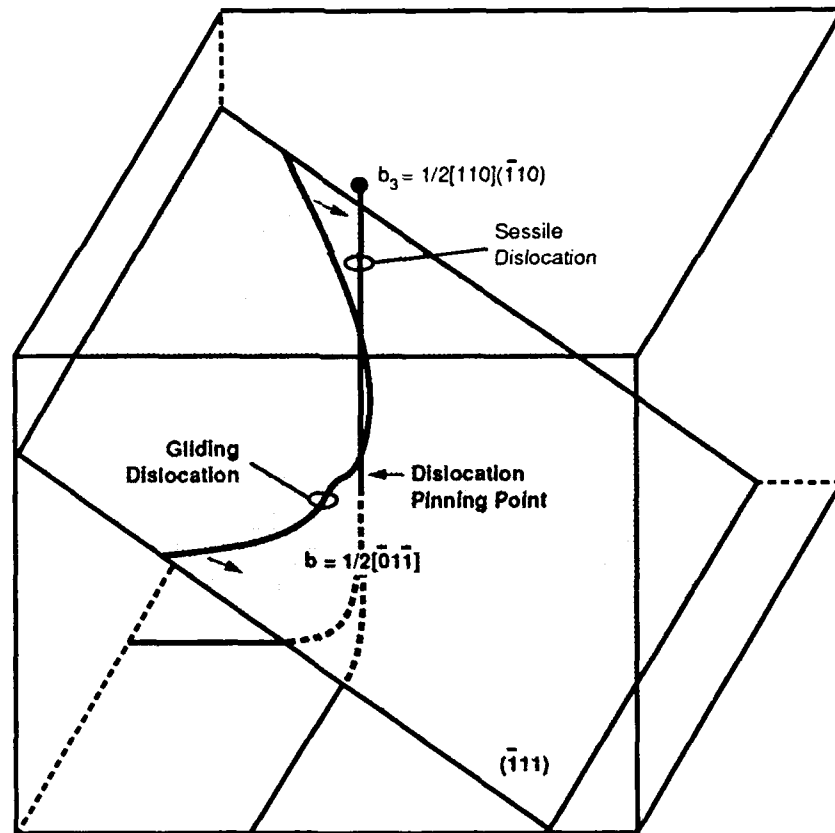
Figure 38
XTEM Micrographs Under Several Imaging Conditions of a Group of Dislocations from the Same Growth Structure as Shown in Figure 37. Note that the dislocations are out of contrast for $\bar{g} = 222$

growth interface and, as such, should experience a glide force as a result of the biaxial misfit stress created by the strained-layer superlattices. However, these dislocations are also observed to thread through the SLSs without deflection, implying that they are also sessile. The length of the dislocation lines relative to the foil thickness suggests that these dislocations are lying close to the $[001]$ direction. Similar to the case described above, these dislocations are not lying on $\{111\}$ habit planes.

The formation of sessile threading dislocations during growth imposes a serious handicap for the removal of dislocations by strain. Not only will these dislocation not be bent to a mismatched interface, but they will act to block the movement of other gliding dislocations. Consider the schematic diagrams shown in Figure 39(a). Figure 39(a) shows two glide dislocations that impinge during the early stages of the growth process to form a resultant threading dislocation. During further epilayer growth this dislocation will replicate in the epilayer, and is not constrained to replicate on a $\{111\}$ -type plane. Figure 39(b) shows the case similar to the experimental case where the dislocation has replicated in a direction close to perpendicular to the growth interface. As such, this dislocation threads through all of the $\{111\}$ planes, which are inclined to the interface plane. As other dislocations glide on these $\{111\}$ planes, i.e., under the influence of a misfit stress such as the SLS, they will be pinned when they intersect the threading dislocation. As a result, benefits of SLSs will not be realized.



(a) Early Stage of Growth



(b) Later Stage of Growth

03198

Figure 39
Schematic Diagram Showing (a) the Generation of a Threading Dislocation from the Interaction of Two Misfit Accommodating Dislocations, and (b) the Blocking Affect of these Dislocations Threading through the Glide Planes of other Dislocations

SECTION V

RECOMMENDATIONS FOR ADDITIONAL STUDY

Results of this research program provide improved understanding of misfit accommodation processes that occur during reduced-area, latticed-mismatched heteroepitaxial growth. Several issues were raised with regard to the effectiveness of reduced growth areas for defect-density reduction during misfit accommodation processes. The following summarizes the most important remaining problems and potential approaches to address them.

A. THE $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ SYSTEM

The use of reduced growth areas for the reduction of defect densities in the $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ materials system has been demonstrated for In compositions up to 25%, and looks very promising for higher In compositions. The ability to grade the composition continuously during growth is a clear advantage for this system, and similar results should be obtained from other materials systems where this is possible. Extension of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ composition-graded growth to the In composition, which is latticed matched to InP ($\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$), requires additional growth development. The primary obstacle to be overcome is the prevention of the breakdown of the two-dimensional to the three-dimensional growth mode. We believe that a combination of linear composition grading, reduced growth temperature, and reduced growth rate is the most promising approach to maintaining two-dimensional growth; migration-enhanced epitaxy (MEE) may also be useful.

B. THE GaAs/Si SYSTEM

Reduced area growth for defect-density reduction in GaAs/Si does not appear to be as promising as with the $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ system. The constraint of the abrupt growth interface is a serious handicap. Threading defect densities, which are generated at the very early stages of growth, are presently too high to realize the benefits of reduced area growth combined with dislocation-bending techniques. These dislocations are formed at the early stages of growth from dislocation interactions. The analysis of the nature of the threading dislocations, which propagate to the surface of the GaAs/Si epilayers, demonstrates that they cannot be substantially reduced using dislocation filtering.

Additional studies should focus on the prevention of the formation of these defects at the early stages of growth. A possibility for study is the use of extremely low growth rates during early stages of reduced area growth, particularly at the growth stage near the misfit dislocation nucleation critical thickness. If the dislocation nucleation rate could be slowed sufficiently during this stage of growth, the gliding dislocations that form the misfit dislocations may have the opportunity to glide across the reduced growth areas without interaction. Again, one means of accomplishing this task might be through the use of the low growth rate technique, migration-enhanced epitaxy.

Another possibility for study is the use of intermediate layers from other materials systems to make the lattice mismatch transition more gradual. Soga et al.³² have reported the growth of GaAs on Si using intermediate layers of AlP , AlGaP , GaP /

GaAs_{0.5}P_{0.5} superlattices, and GaAs_{0.5}P_{0.5}/GaAs superlattices. They found improved x-ray rocking curve linewidths and photoluminescence intensity; however, a study of the defect structure was not discussed. The use of Ge_xSi_{1-x} alloy grading is also another possibility for distributing the mismatch.

REFERENCES

1. M.A. Pollack, *Materials Science and Engineering*, **B6**:233 (1990).
2. J.W. Matthews, A.E. Blakeslee and S. Mader, *Thin Solid Films*, **33**:253 (1976).
3. D.B. Fenner, D.K. Biegelsen, B.S. Krusor, F.A. Ponce and J.C. Tramontana, *Mat. Res. Soc. Symp. Proc.*, **159**:15 (1990).
4. M.S. Abrahams, C.J. Buicocchi and G.H. Olsen, *Journal of Applied Physics*, **46**(10):4259 (1975).
5. M.M. Al-Jassim, R.K. Ahrenkiel, J.M. Olson and S.M. Vernon, MRS Proceedings 1990.
6. C.M. Serrano and C.A. Chang, *Applied Physics Letters*, **39**(10):808 (1981).
7. S.M. Bedair, T.P. Humphreys, N.A. El-Masry, Y. Lo, N. Hamaguchi, C.D. Lamp, A.A. Tuttle, D.L. Dreifus and P. Russell, *Applied Physics Letters*, **49**(15):942 (1986).
8. B.W. Dodson, *Journal of Electronic Materials*, **19**:6:503 (1990).
9. Y. Watanabe, M. Uneta, Y. Kadota and Y. Ohmachi, *Journal of Electronic Materials*, **19**(3):219 (1990).
10. E.A. Fitzgerald, G.P. Watson, R.E. Proano, D.G. Ast, P.D. Kirchner, G.D. Pettit and J.M. Woodall, *Journal of Applied Physics*, **65**(6):2220 (1989).
11. E.A. Fitzgerald, *Jour. Vac. Sci. Technol.*, **B7**(4):782 (1989).
12. S. Guha, A. Madhukar, K. Kaviani and R. Kapre, *Jour. Vac. Sci. Technol.*, **B8**(2):149 (1990).
13. R.J. Matyi, H. Shichijo and H.L. Tsai, *Jour. Vac. Sci. Technol.*, **B6**(2):699 (1988).
14. M.N. Charasse, B. Bartenlian, J.P. Hirtz, A. Peugeot, J. Chazelas and G. Amendola, *J. Electronic Materials*, **19**(6):567 (1990).
15. D.B. Noble, J.L. Hoyt, C.A. King, J.F. Gibbons, T.I. Kamins and M.P. Scott, *Appl. Phys. Lett.*, **56**(1):51 (1990).
16. R.J. Matyi, H. Shichijo, T.M. Moore and H.L. Tsai, *Appl. Phys. Lett.*, **51**(1):18 (1987).
17. N. Chand, J.P. van der Ziel, J.S. Weiner, A.M. Sergent, A.Y. Cho and K.A. Grim, *Appl. Phys. Lett.*, **53**(3):227 (1988).
18. W.T. Tsang and A.Y. Cho, *Appl. Phys. Lett.*, **32**(8):491 (1978).
19. S. Nagata and T. Tanaka, *Jour. Appl. Phys.*, **48**(3):940 (1977).
20. W.T. Tsang and A.Y. Cho, *Appl. Phys. Lett.*, **30**(6):293 (1977).
21. J.P. van der Ziel, N. Chand and J.S. Weiner, *Mat. Res. Soc. Symp. Proc.* **145**:317 (1989).
22. E.A. Beam III, Y.C. Koa and J.Y. Yang, (submitted to *Applied Physics Letters*).
23. J.W. Matthews, S. Mader, and T.B. Light, *Journal of Applied Physics*, **41**:3800 (1970).

24. S.N.G. Chu, S. Nakahara, R.F. Karlicek, K.E. Strege, D. Mitcham and W.D. Johnston, Jr., *Journal of Applied Physics*, **59** (10):3441 (1986).
25. P.R. Berger, K. Chang, P. Bhattacharya, J. Singh and K.K. Bajaj, *Applied Physics Letters*, **53** (8):684 (1988).
26. Y.C. Chen, P.K. Bhattacharya and J. Singh, *Applied Physics Letters*, **57** (7):692 (1990).
27. E.A. Fitzgerald, D.G. Ast, P.D. Kirchner, G.D. Pettit and J.M. Woodall, *Journal of Applied Physics*, **63** (3):693 (1988).
28. E.A. Beam III, S. Mahajan and W.A. Bonner, *Materials Science and Engineering B*, **7**:83 (1990).
29. Y.C. Kao, H.Y. Liu, H.L. Tsai, W.M. Duncan, T.S. Kim and H. Shichijo, *Jour. Vac. Sci. Technol.*, **B8** (2):250 (1990).
30. S. Mahajan, V.G. Keramidas and W.A. Bonner, *Jour. Electrochem. Soc.* **129** (7):1556 (1982).
31. J.P. Hirth and J. Lothe, *Theory of Dislocations*, Wiley, New York, 1982.
32. T. Soga, S. Hattori, S. Sakai, M. Takeyasu, and M. Umeno, *J. Appl. Phys.*, **57**(10):4578 (1985).